



# HIL and RCP capabilities of real time digital simulators for MMC and other power converter applications

**Wei Li, OPAL-RT**

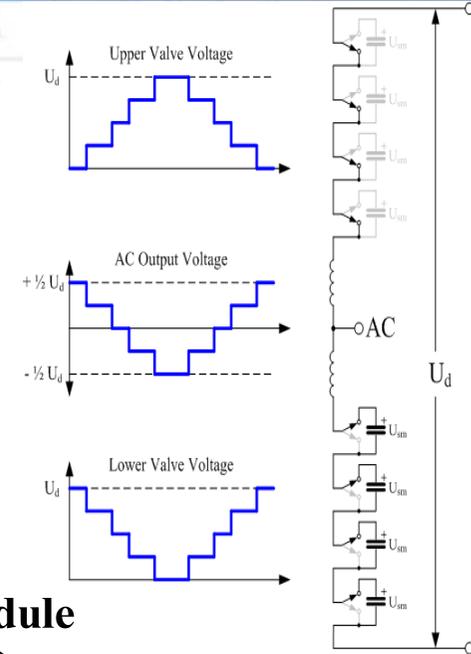
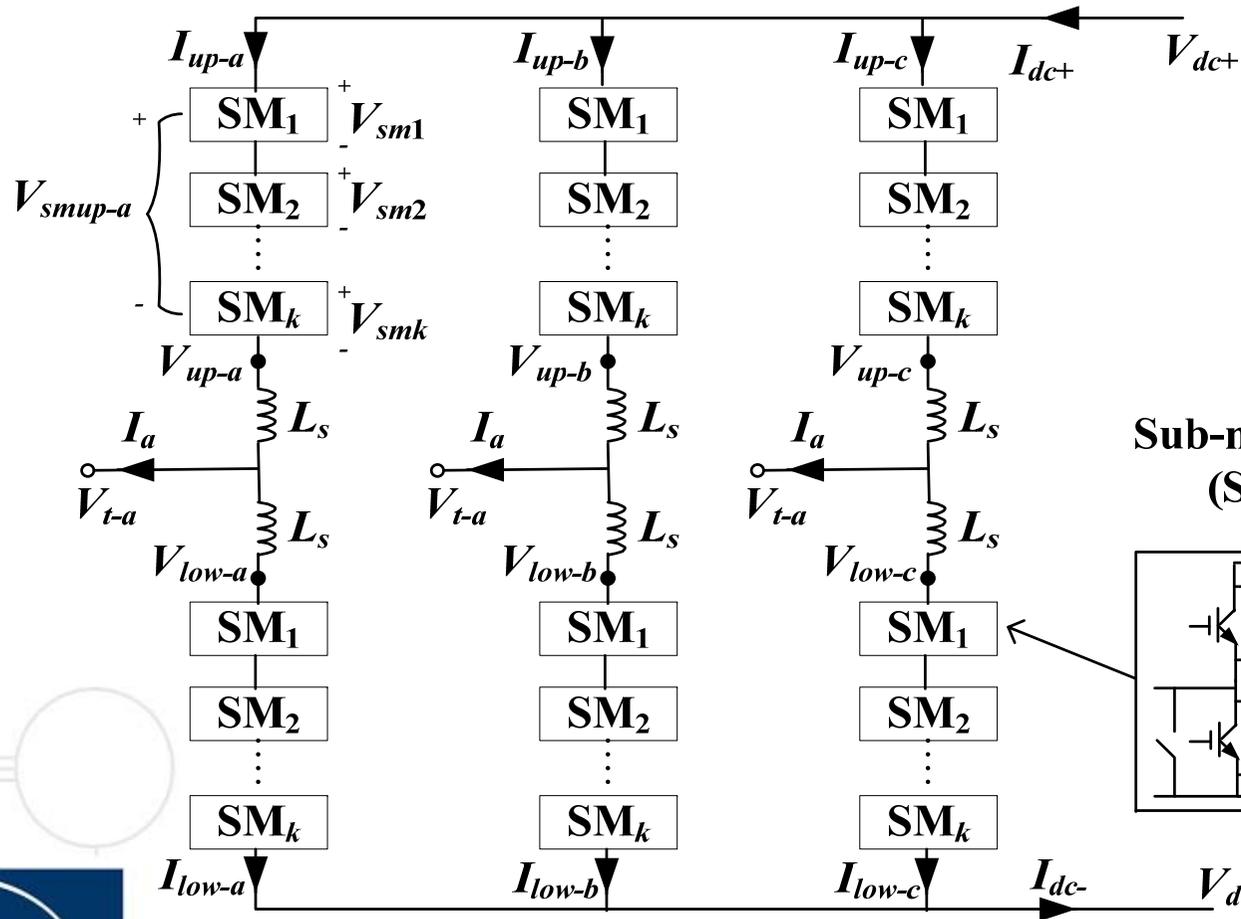
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- ❖ MMC characteristics & advantages
- ❖ MMC projects and challenges
- ❖ Solutions to
  - Real time simulation of MMC systems
  - HIL test bench for MMC Control and protection system validation
- ❖ Industrial applications
- ❖ Conclusions

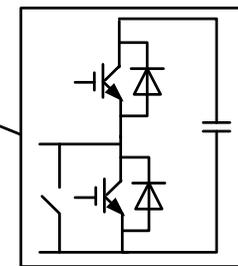


# MMC HB ac-dc Converter

## ❖ Modular Multilevel Converter

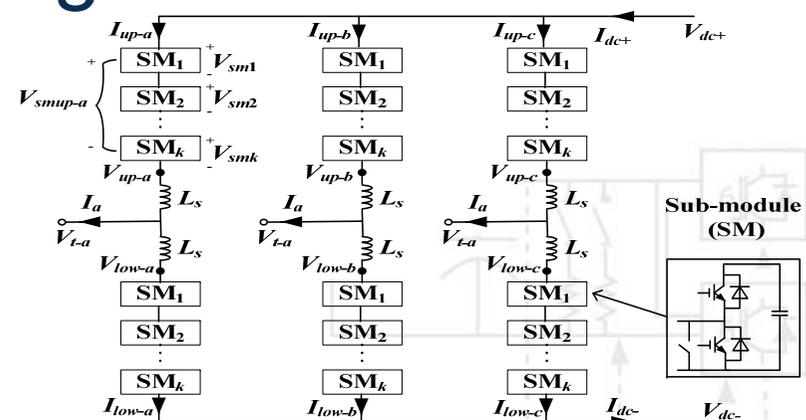


Sub-module (SM)



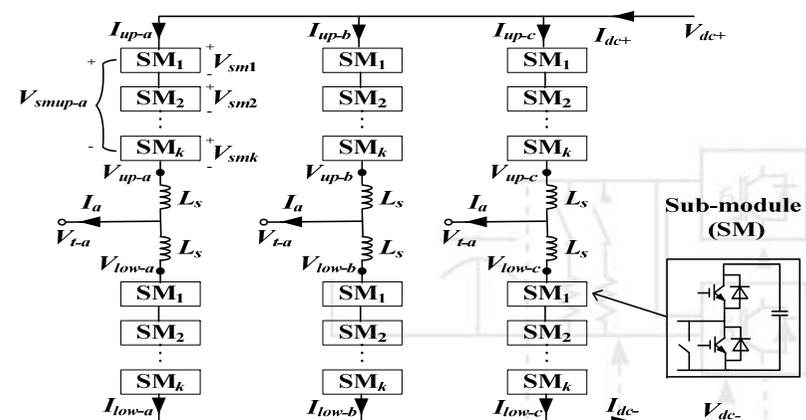
# MMC Characteristics

- ❖ Commutating inductors are in arms
- ❖ Arm currents are continuous
- ❖ Capacitors in each cell (energy storage in MMC)
- ❖ SM capacitor voltage has to be balanced (on a larger time scale)
- ❖ Circulation current among arms



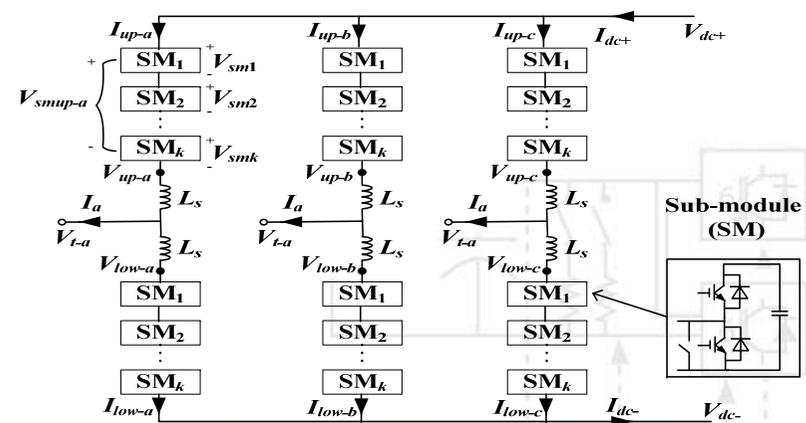
# MMC Advantages

- ❖ Reduced stress on converter and grid component
- ❖ Low switching frequency – reduced switch losses
- ❖ Low ac harmonic content – no need for a filter
- ❖ Continuous currents in MMC arm and DC link - dc link capacitor omitted
- ❖ Fast recovery from AC-bus short-circuit (Better fault ride-through capacity )



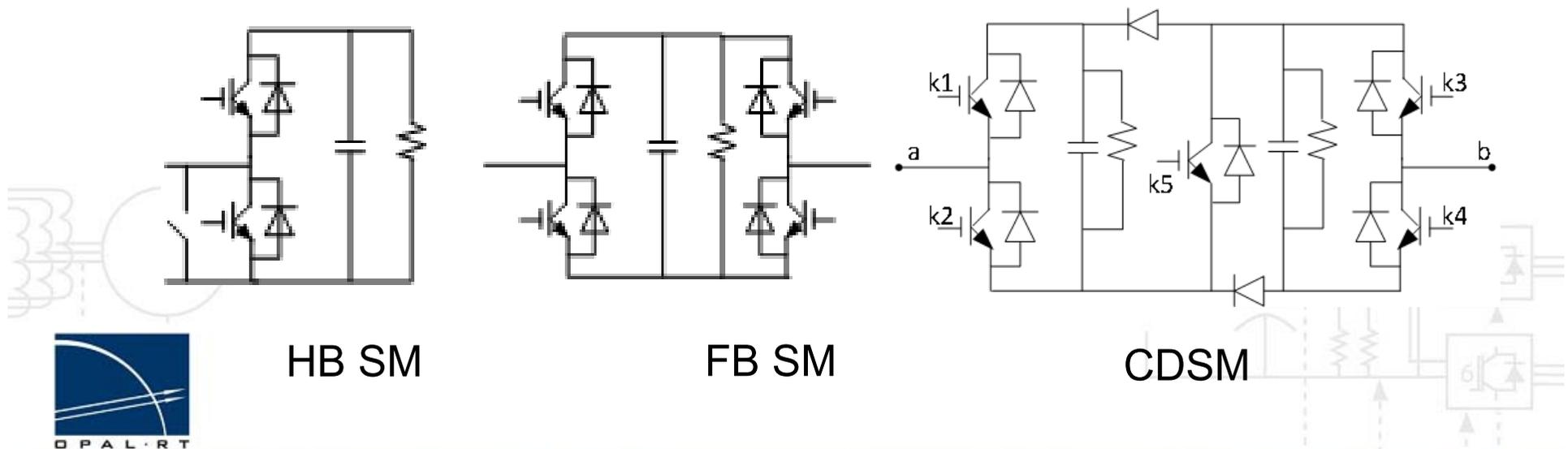
# MMC Advantages (continued)

- ❖ Fast recovery from DC-bus short-circuit, but DC breaker or FB or CDSM topologies are needed
- ❖ Improved reliability due to modular design and redundancy in SM- system can remain operating for a certain period even when a few SM are out of order
- ❖ Can feed loads without any generators (no limit on short-circuit ratio)
- ❖ Easy start-up
- ❖ Smaller foot print

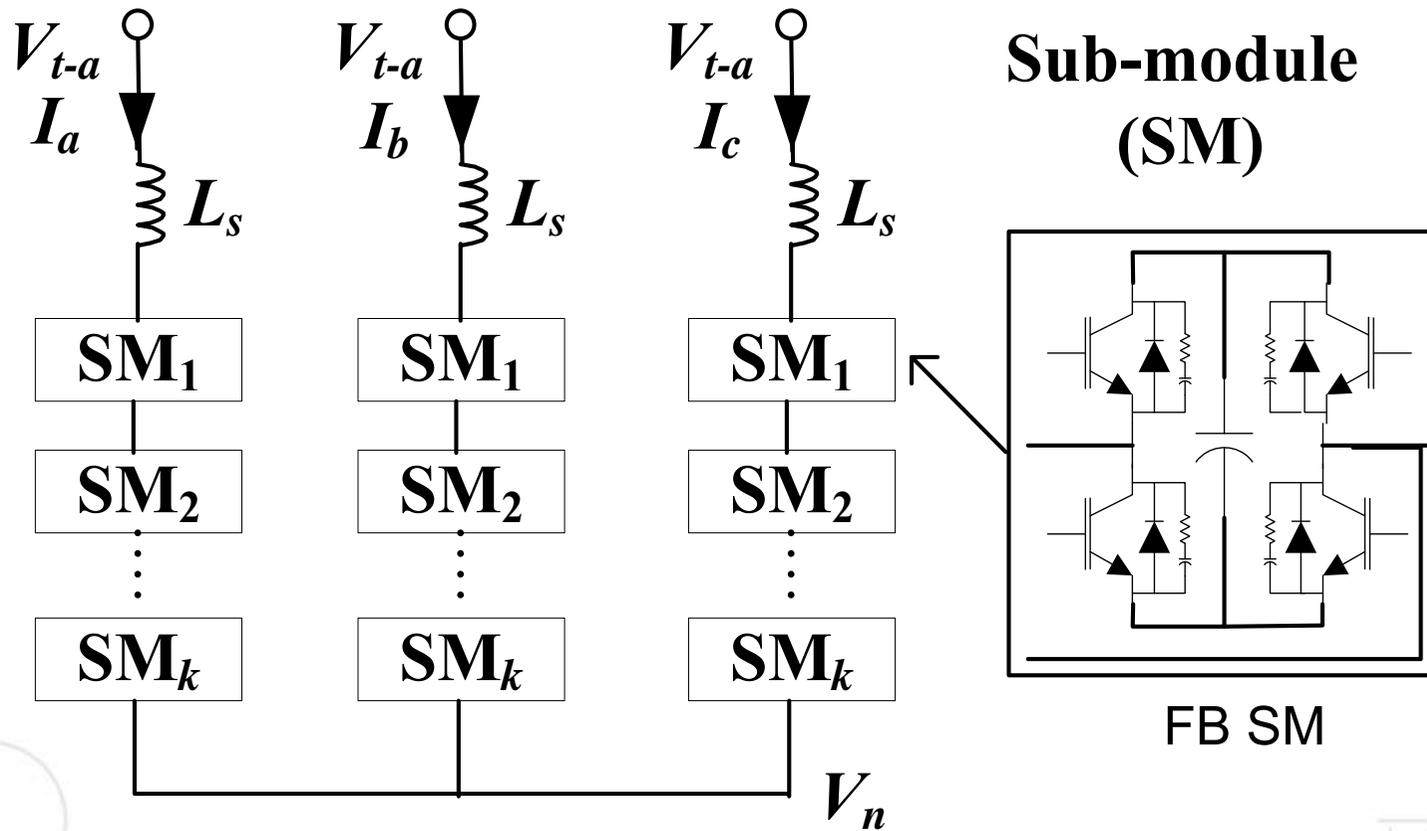


# MMC and Sub-module

- ❖ Sub-module (SM) topologies
  - Half-bridge (HB): with 2 IGBT and 1 Capacitor
  - Full-bridge (FB): with 4 IGBT and 1 Capacitor
  - Clamp Double (CD): with 5 IGBT and 2 Capacitors
  - others



# MMC FB SM STATCOM



# Recent MMC HVDC projects in China



Nanhui, 2011

Zhoushan, 2014

Xiamen 2015 (State grid): Bi-pole MMC  $\pm 320$  kV, 1000MVA HVDC for city power supply

Nanao, 2013

Luoping (CSG) : MMC-LCC combined back-to-back  $\pm 350$  kV, 2000 MVA HVDC Links (one 1000 MVA MMC link and one 1000 MVA LCC link) for asynchronous network coupling

- ★ MMC Project in operation
- MMC Project under construction



# Recent MMC HVDC projects in China

Project	Year in operation	Nb. of terminals	Nb. of SM per valve	Rated DC Voltage	Capacity	Application
Nanhui	2011	2	50	60 kV	18 MVA	Wind Energy Integration
Nanao	2013	3	200	320 kV	200 MVA	Wind Energy Integration
Zhoushan	2014	5	250	400 kV	400 MVA	Power supply for islands
Luoping	2016	2	400	$\pm 350$ kV	1 GVA	Asynchronous Networks Coupling
Xiamen	2015	2	400	$\pm 320$ kV	1 GVA	Power supply for large cities

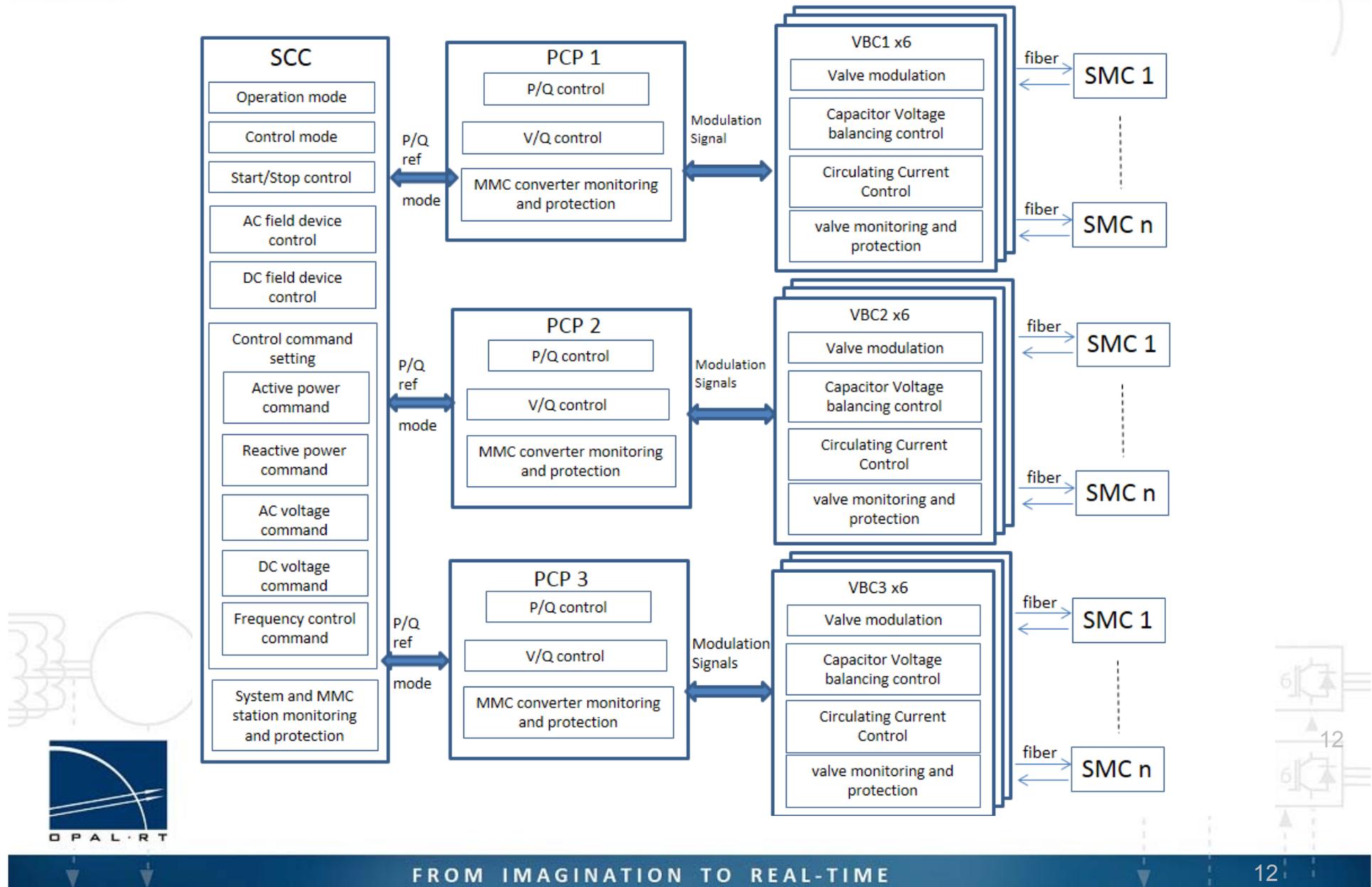


# MMC challenges

- ❖ New technologies and little engineering experience from existing projects
- ❖ Complex control and protection systems
  - Which could be supplied by different manufacturers in multi-terminal systems
- ❖ Expensive to make and maintain a physical test bench



# Challenges – Structure of MMC C&P system

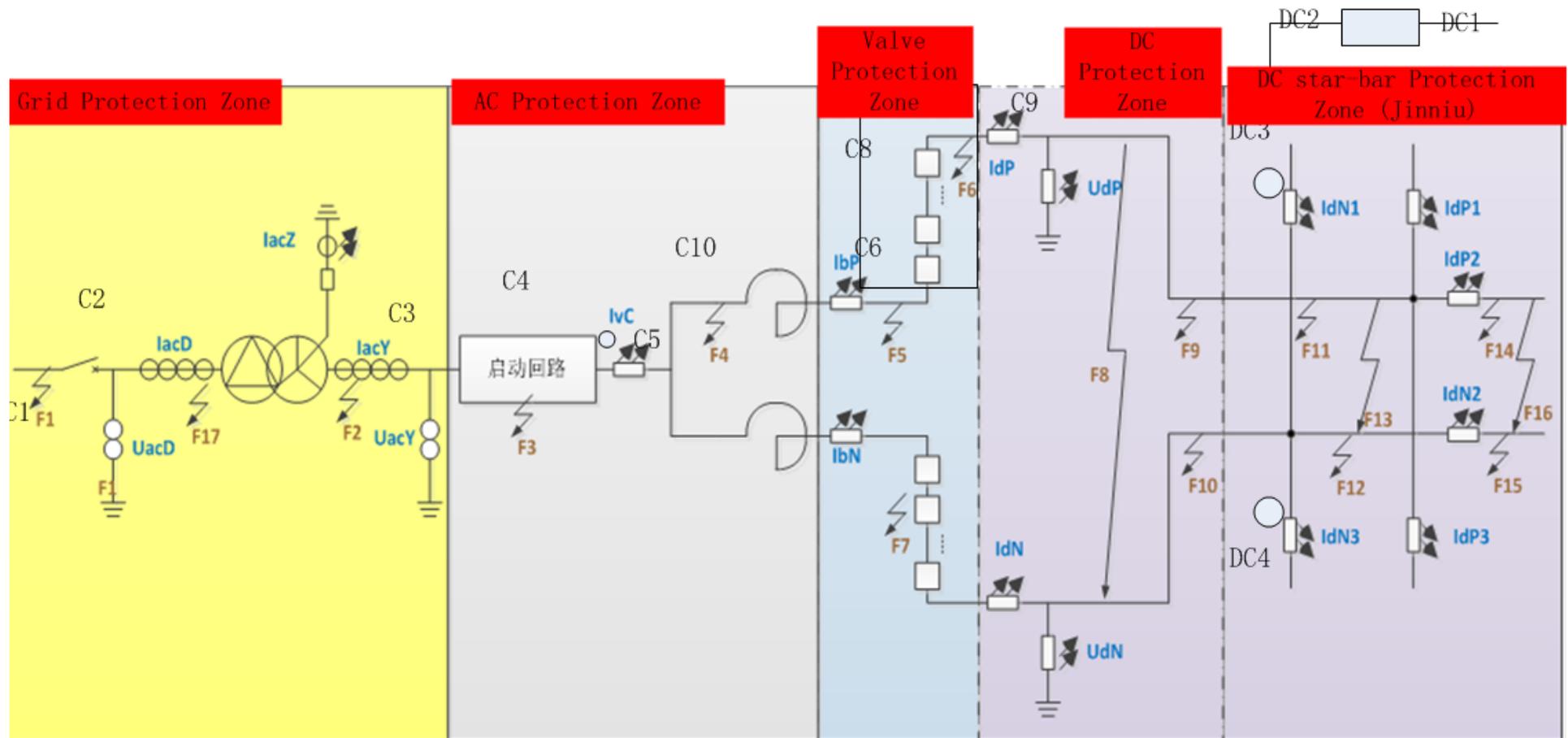


# Challenges – Test matrix and sequence

STATCOM operation	AC & HVDC Operation	Pure DC Operation
<ul style="list-style-type: none"><li>• Auto Start sequence</li><li>• Power step command</li><li>• PCP redundancy</li><li>• Internal communication failure</li><li>• AC faults</li><li>• DC faults</li><li>• Valve faults</li></ul>	<ul style="list-style-type: none"><li>• Auto Start sequence</li><li>• Power step command</li><li>• PCP redundancy</li><li>• Operation with and without substation communication</li><li>• AC faults</li><li>• DC faults</li><li>• Valve faults</li></ul>	<ul style="list-style-type: none"><li>• Auto Start sequence</li><li>• Power step command</li><li>• PCP redundancy</li><li>• Operation with and without substation communication</li><li>• AC faults</li><li>• DC faults</li><li>• Valve faults</li></ul>

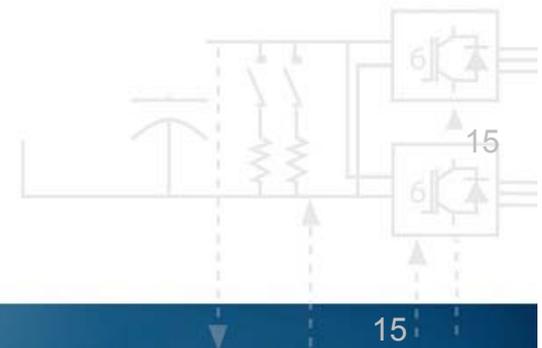


# Challenges – AC and DC faults assignment



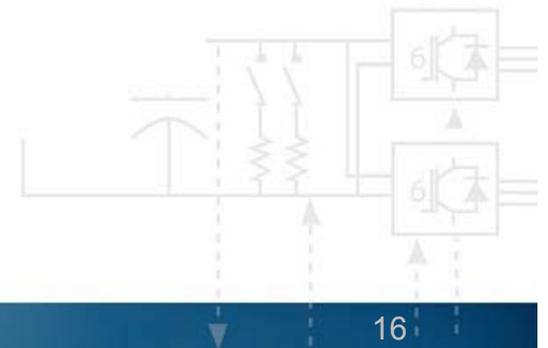
## MMC challenges and solution

- ❖ Solutions to validation of MMC C&P systems:  
Hardware-in-the-loop (HIL) test bench
  - Lower cost
  - Shorter time for R&D cycle and validation test
  - Wider range of tests: steady states, transients, & faults



# Challenges for real time simulation of MMC

- ❖ challenges for real time simulation and HIL test bench
  - Large number of components
  - Large number of switches, frequent change of switch states
  - Non-linear elements, e.g. MOV
  - Large number of I/Os to interface with controllers



# Solutions to real time simulation of MMC

- ❖ **Circuit simplification** [1,2]
  - Using one equivalent capacitor for a valve. Loss of details.
- ❖ **Norton equivalent using Dommel's algorithm**[4,5]
  - Dommel's algorithm[3]: switch  $\leftarrow R_{\text{on/off}}$ ,  $C \leftarrow R//I_s$ .
- ❖ **Norton equivalent + SSN parallel calculation**[7]
  - SSN[6]: state space nodal method for parallel calculation.
- ❖ **Surrogate networks with Thevenin equivalent**[8]
  - SM grouped according to states (insert, bypass, block)
- ❖ **General MMC valve equivalent circuit** [9]
  - for all SM topologies, parallel calculation



# Solutions to real time simulation of MMC

## ❖ Circuit simplification [1,2]

- Using one equivalent capacitor for a valve. Loss of details.

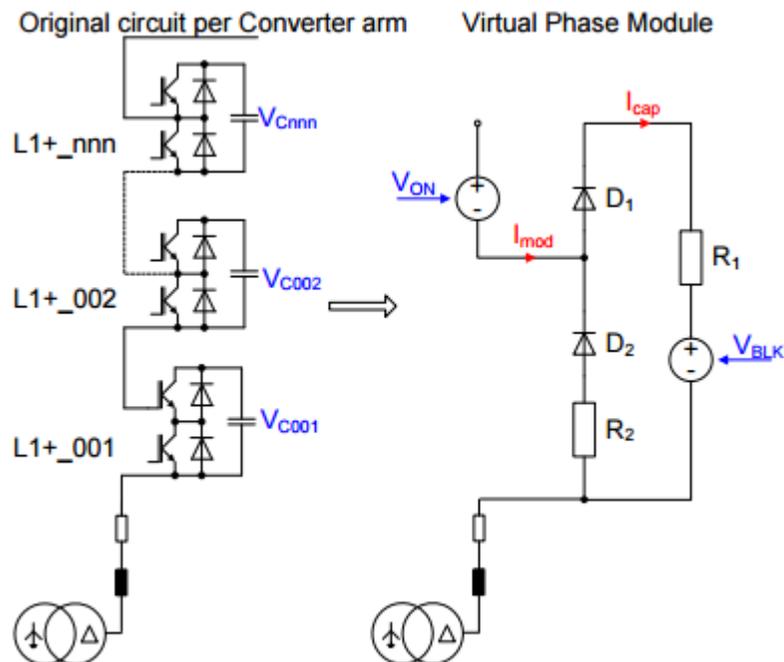


Fig. 2. Original electric circuit and Virtual Phase module electric circuit

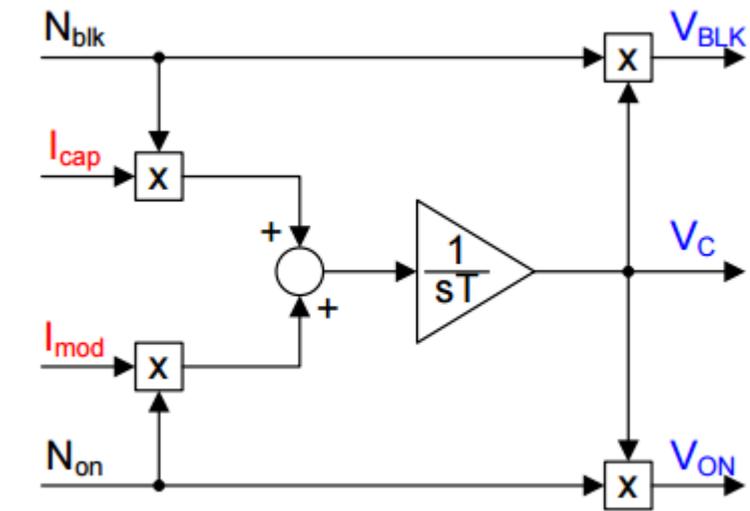


Fig. 3. Capacitor Voltage Calculation

Figures from reference [2] by O. Venjakob et al.



# Solutions to real time simulation of MMC

- ❖ Norton equivalent using Dommel's algorithm[4,5]
  - Dommel's algorithm[3]: switch  $\leftarrow R_{\text{on/off}}$ ,  $C \leftarrow R//I_s$ .

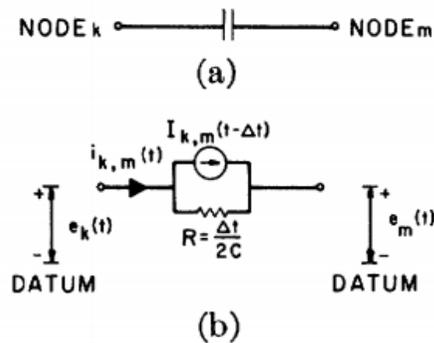


Fig. 3. (a) Capacitance. (b) Equivalent impedance network.

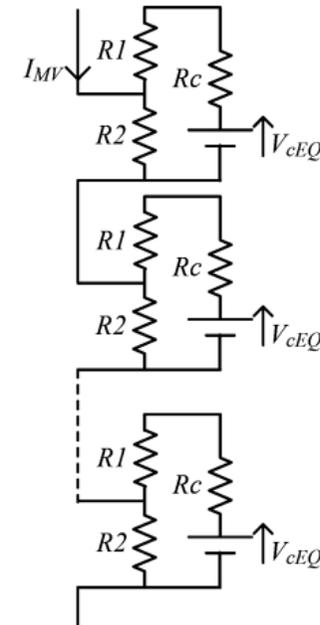


Fig. 7. Equivalent circuit representation for a multivalve.



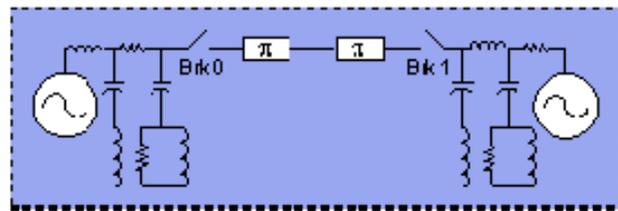
Fig.3. from reference [3] by H. W. Dommel.

Fig.7. from reference [4] by U. N. Gnanarathna et al.

# Solutions to real time simulation of MMC

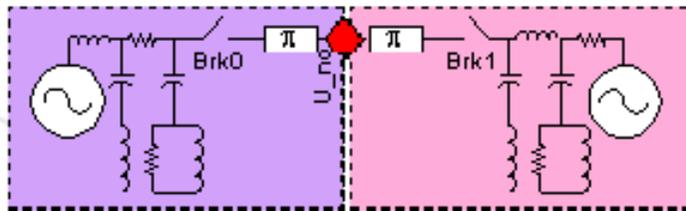
- ❖ Norton equivalent + SSN parallel calculation[7]
  - SSN[6]: state space nodal method for parallel calculation.

State space method with  $x$  states



$$\dot{x}_{k+1} = A_k x_k + B_k u_{k+1} \quad \text{matrices } k=1..M$$

SSN method with 2 groups of  $x/2$  states each



$$\dot{x}_{k+1} = \begin{bmatrix} A1_m & & & \\ & A2_n & & \\ & & B1_m & \\ & & & B2_n \end{bmatrix} x_k + \begin{bmatrix} B1_m \\ B2_n \end{bmatrix} u_{k+1} \quad \text{matrices } m=1..M, n=1..N$$

$$U_{NO_{k+1}} = Y_{3,3} U_{NO_{k+1}}$$

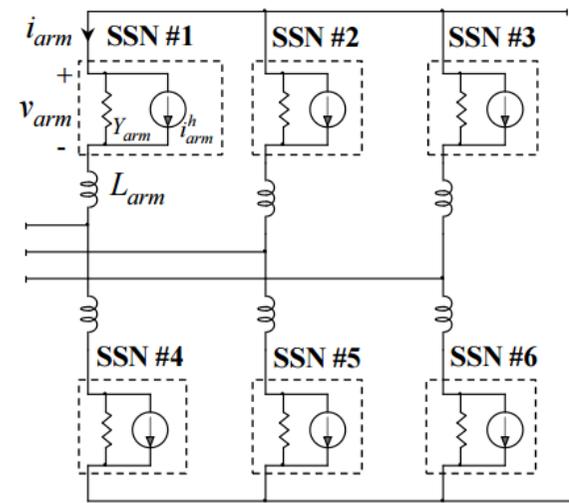


Fig. 6 SSN-MMC model

Figures from reference [7] by H. Saad et al.



# Solutions to real time simulation of MMC

- ❖ Surrogate networks with Thevenin equivalent[8]
  - SM grouped according to states (insert, bypass, block)

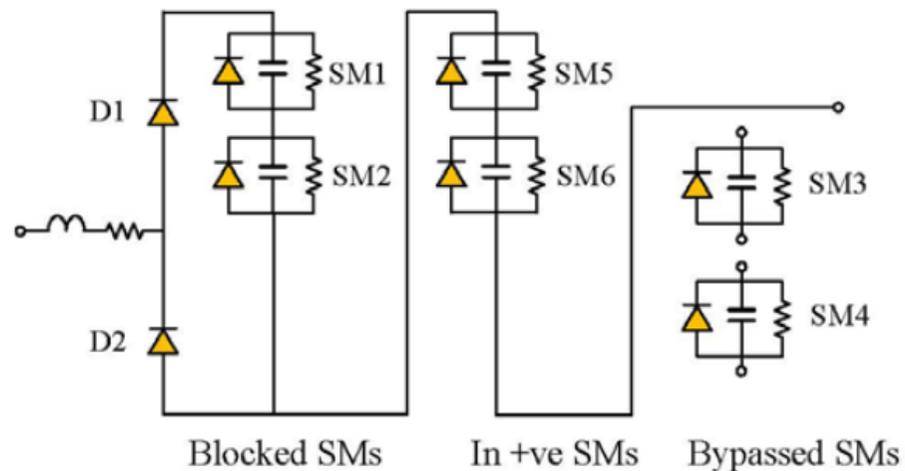


Figure 2. Half-bridge surrogate network topology

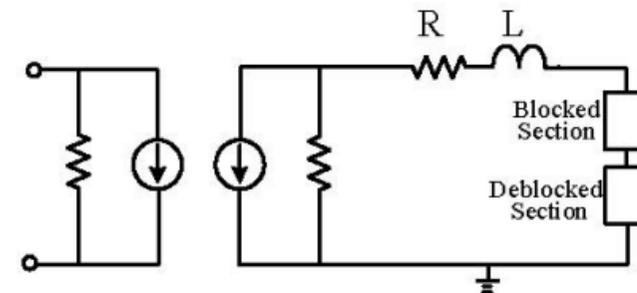
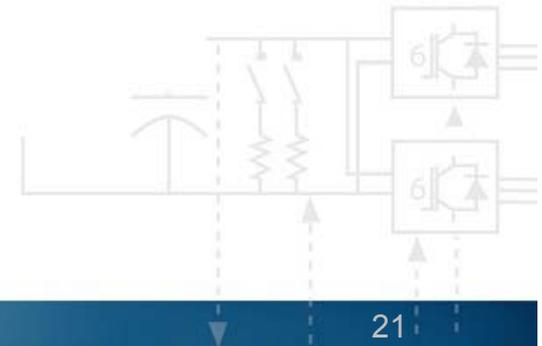


Figure 5. The T-Line Interface in the surrogate network topology

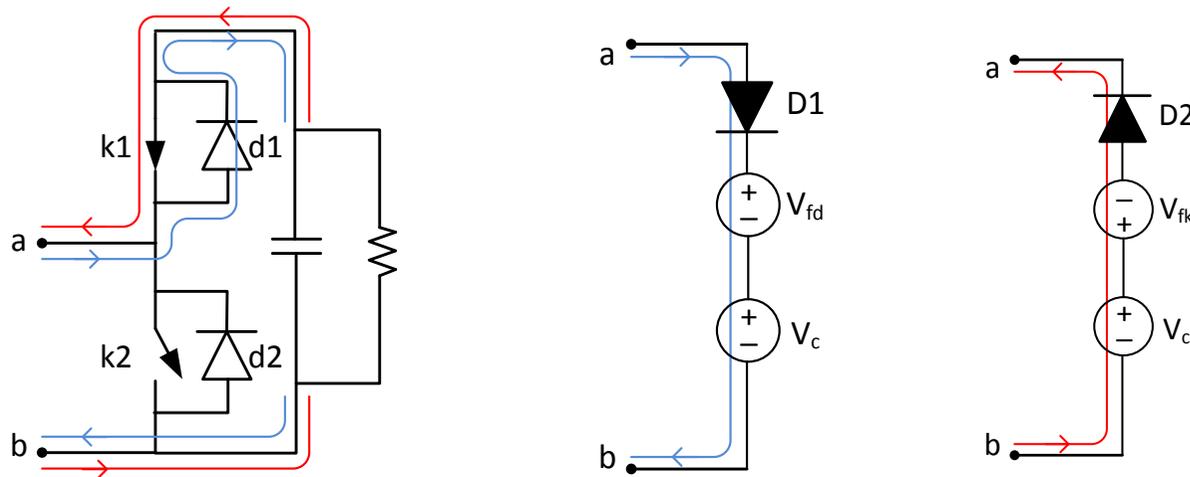


Figures from reference [8] by T. L. Maguire et al.



# OPAL-RT Solution for MMC Simulation

- ❖ General MMC valve equivalent circuit [9]
  - for of all SM topologies, parallel calculation

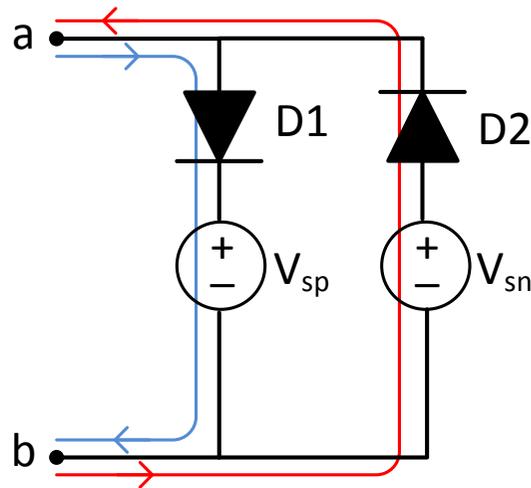


(a) HB SM in insert mode and equivalent circuits for (b) positive and (c) negative current directions



# OPAL-RT Solution for MMC Simulation

- ❖ General MMC valve equivalent circuit [9]
  - for of all SM topologies, parallel calculation



A general SM equivalent circuit for all operating conditions

Table I Source voltages in HB SM Equivalent Circuit

Mode	k1	k2	$V_{sp}$	$V_{sn}$
Insert	1	0	$V_c + V_{fd}$	$V_c - V_{fk}$
Bypass	0	1	$V_{fk}$	$-V_{fd}$
Diode	0	0	$V_c + V_{fd}$	$-V_{fd}$
Fault	1	1	$V_{fk}$	$-V_{fk}$

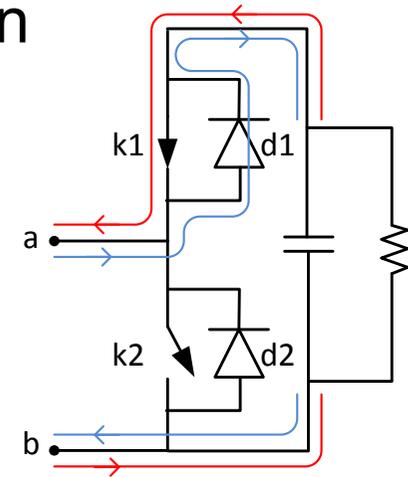


# OPAL-RT Solution for MMC Simulation

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  - for of all SM topologies, parallel calculation

Capacitor voltage:

$$V_c(t + T_s) = V_c(t) + \frac{T_s}{C_{SM}} \left( k(t) i_{val}(t) - \frac{V_c(t)}{R_{disc}} \right)$$



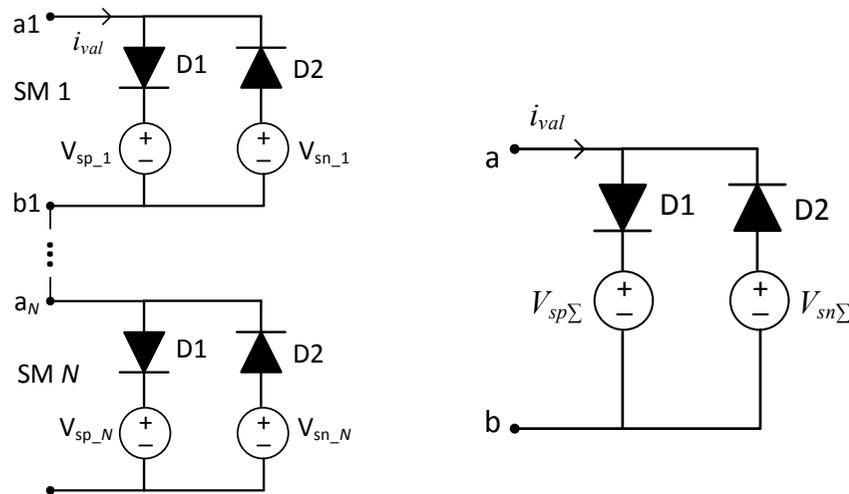
VARIABLE  $k$  IN CAPACITOR VOLTAGE EQUATION FOR HB SM

Mode	k1	k2	Valve current direction	k
Insert	1	0	either	1
Bypass	0	1	either	0
Diode	0	0	positive	1
			negative	0

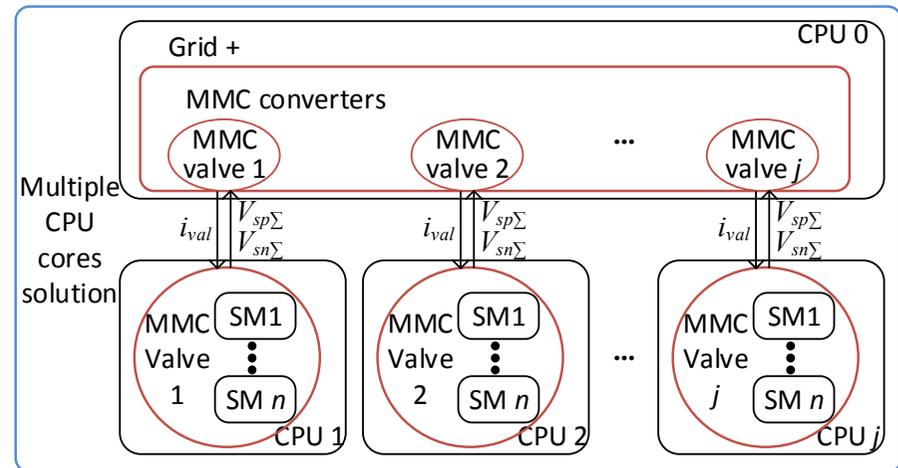


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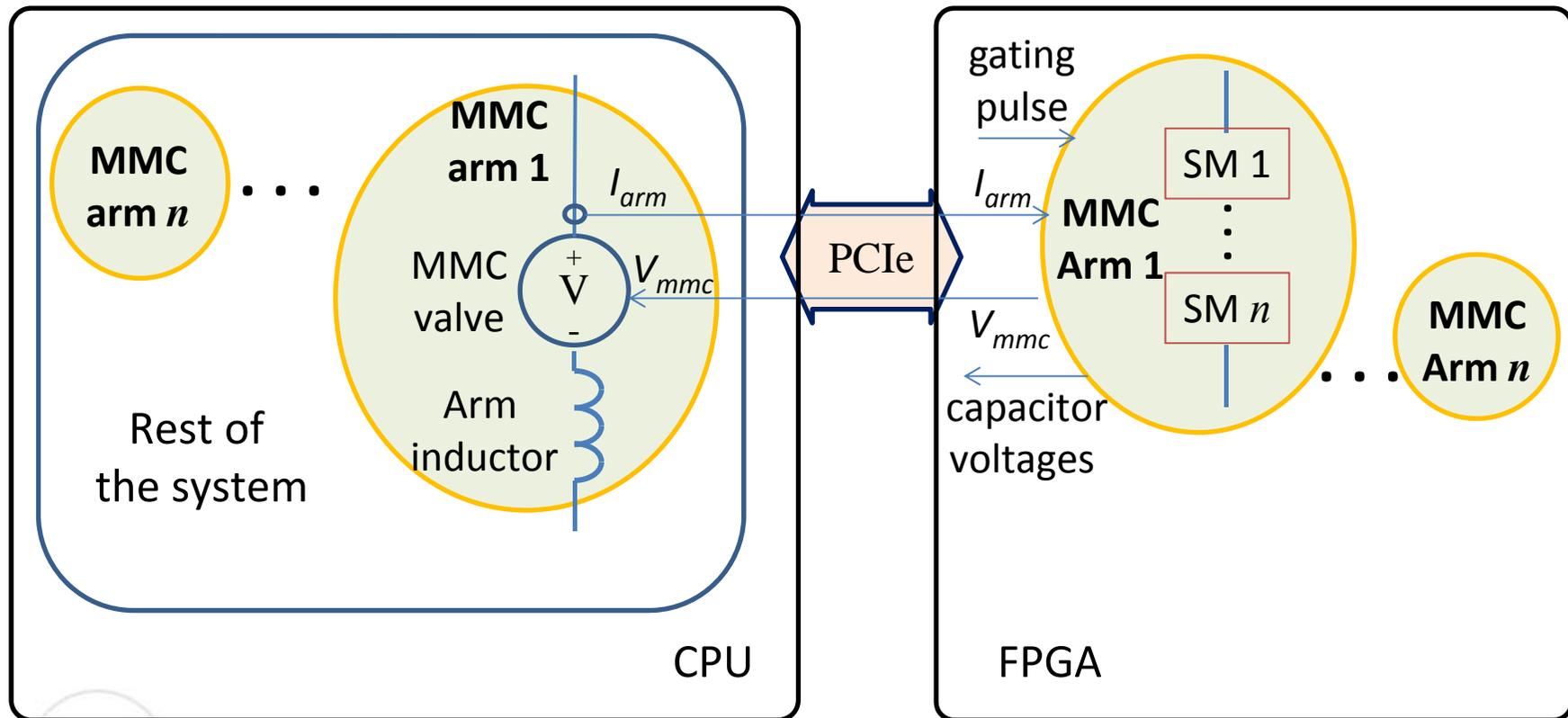
Equivalent circuits of (a) a stack of SM and (b) an MMC valve for all operating conditions.



Parallel solving grid and MMC valves



# Multi-rate MMC Model

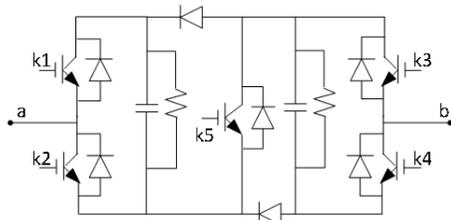
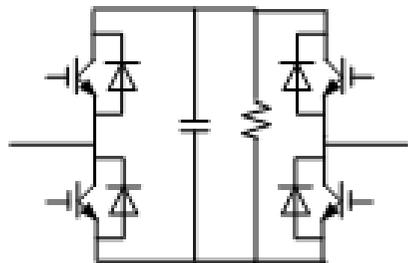
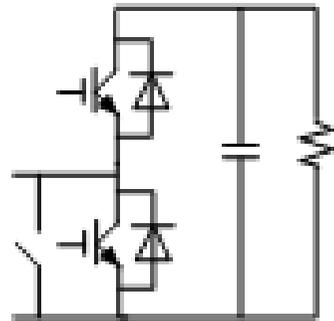


# OPAL-RT Solution for MMC Simulation

- ❖ **Multi-rate MMC model in FPGA ( $T_{\text{fpga}}=250$  ns) and CPU (Ts: tens of  $\mu\text{s}$ )**
- ❖ **Optional MMC models on CPU (25  $\mu\text{s}$ )**
- ❖ Different SM topologies, HB, FB, CDSM, and other
- ❖ For HVDC, STATCOM, other Applications.
- ❖ Real time or fast simulation.
- ❖ HIL and RCP (rapid control prototyping)
- ❖ Hardware IO: Copper wiring or optical fibers
- ❖ Example MMC controller
- ❖ In RT-LAB or Hypersim platform



# Detailed Model of Individual SM



Each of Individual SM is simulated

yes

In each SM

Each capacitor voltage controlled individually

yes

Discrepancy of SM capacitance values

yes

Discharge resistance is simulated

yes

Resolution of firing signal

250 ns

Simulation of dead time

yes

Cell short circuit and other faults

yes

Forward voltage of diodes

yes

Diode non linearity

no

Dynamic of IGBT and diode  
Turn-on and -off

Not yet

# Implementation MMC model in FPGA

- ❖ Small calculation time step of 250 ns
- ❖ Large number of SM
  - up to 256 SM/valve \* 6 valve in VIRTEX 6 (OP7000, ML605) and 256 SM/valve \* 6 valve \* 2 converter in Kintex 7 (OP4500)
  - 512 SM \* 6 valve \* 2 or more converters in VIRTEX 7 (op7020, op5607) (6,000 cells total) including 16 SFP (5 Gbits/s) with AURORA interface protocol
- ❖ MMC VBC (low-level controller) and communication protocol could be implemented in same FPGA
- ❖ Support multiple FPGAs for HVDC grids



# Implementation MMC in FPGA (continued)

- ❖ CPU resources is free to simulate larger AC network because no CPU resource is required
  - to calculate the MMC cell models
  - to manage I/O data communication with external controller
- ❖ Individual control of each IGBT and SM capacitor voltage
- ❖ Providing SM  $V_{cap}$  debugging mode to help user developing their controller
- ❖ Supporting both RT-LAB and Hypersim Platform



# Implementation MMC Model in CPU

- ❖ Useful for off-line simulation of simple system (no FPGA needed) and algorithm development with SIMULINK
- ❖ Supporting MMC HB, FB, and CDSM topologies
- ❖ Unlimited number of SM per valve
- ❖ Several CPU cores are used to calculate the MMC and grid models
- ❖ 1 CPU can solve 300 SM with a time step of  $25\mu\text{s}$
- ❖ Providing SM  $V_{\text{cap}}$  debugging mode to help user developing their controller



# Connectivity with External Controller

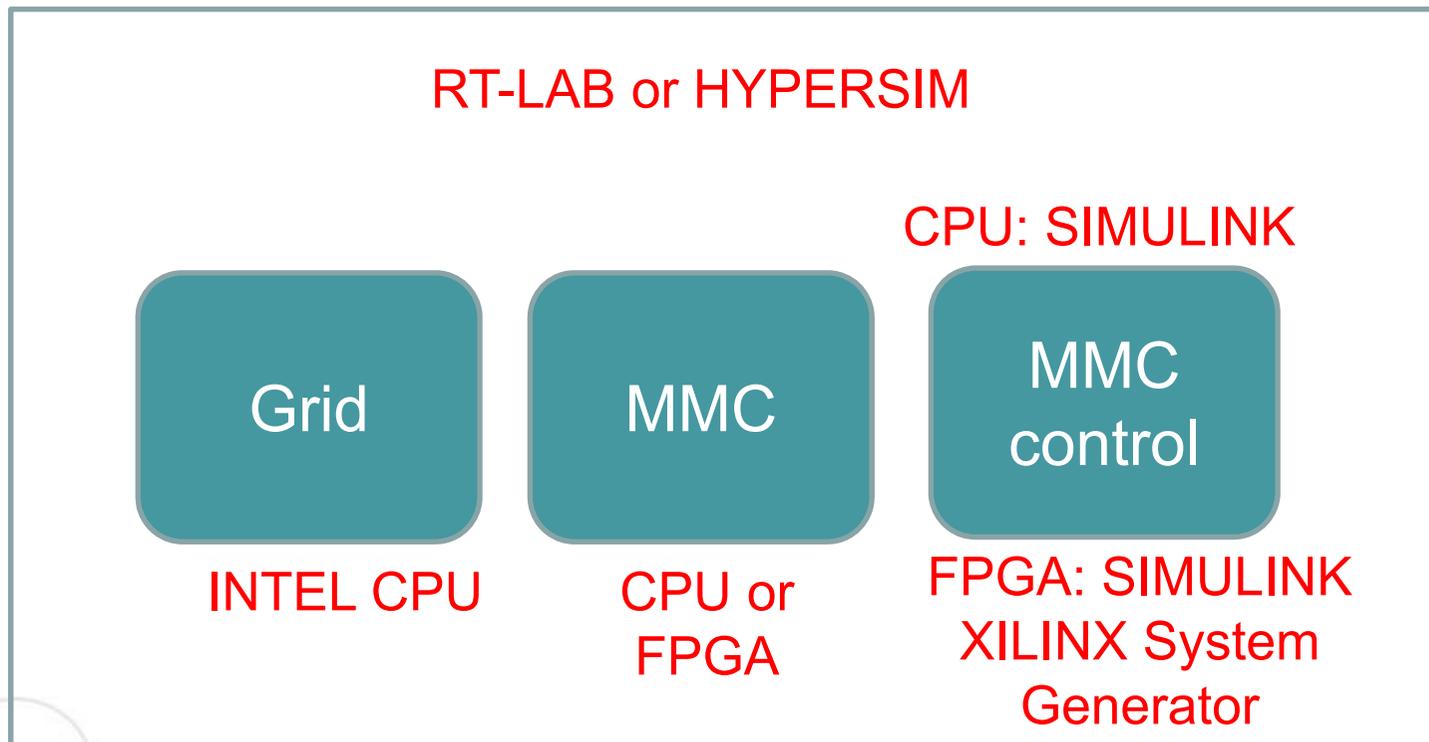
- ❖ Analog and digital I/Os for  $V_{cap}$ , currents, and gating pulses
- ❖ SFP optical fiber with Aurora protocol at 1 to 5 Gbits/s (16 links per VIRTEX-7 FPGA)
- ❖ SFP optical fiber with Gigabit Ethernet protocol
- ❖ Updating interval at a few  $\mu\text{s}$  depending on the number of optical fibers, number of cells and controller manufacturer requirements



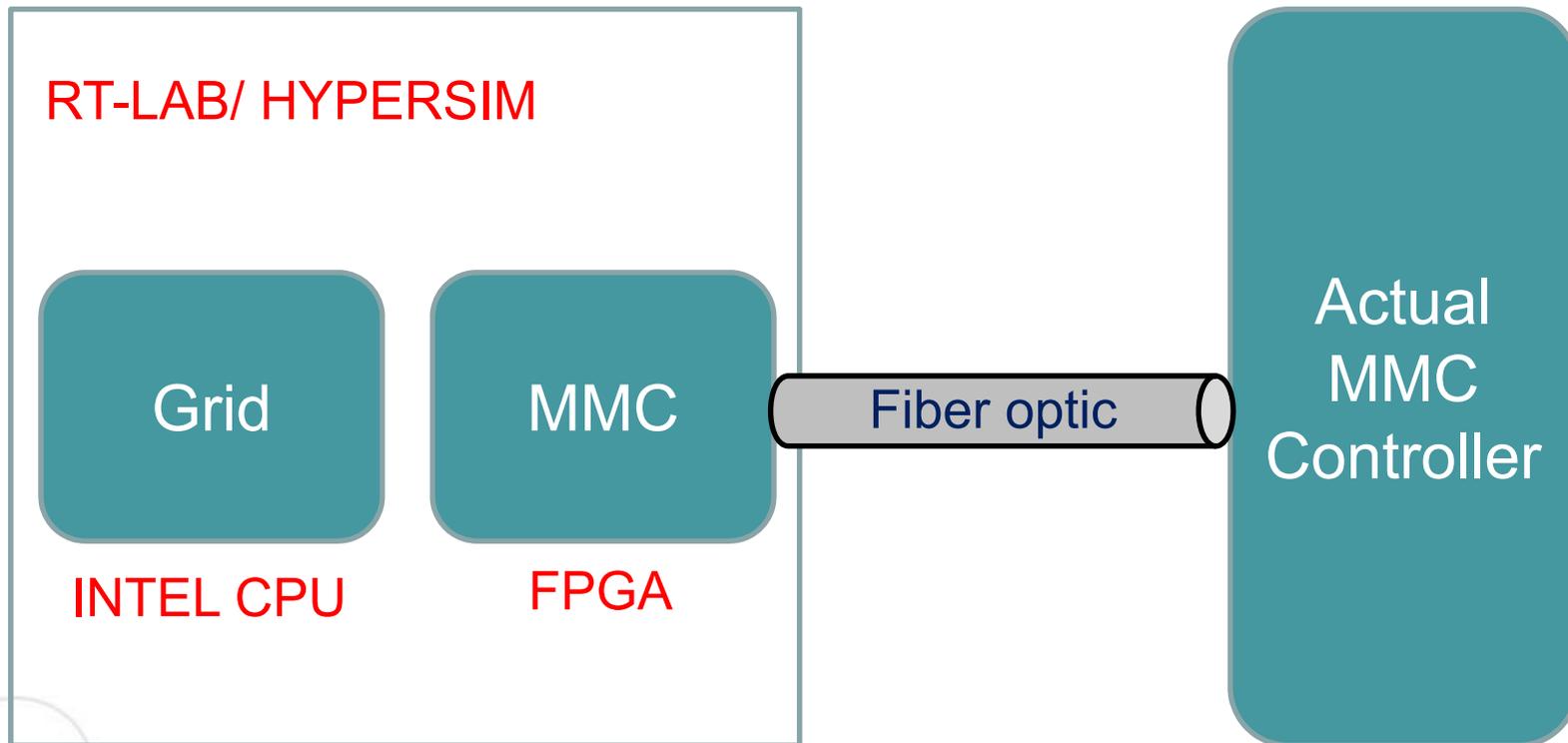
The small form-factor pluggable (SFP) is a compact, hot-pluggable transceiver used for both telecommunication and data communications applications



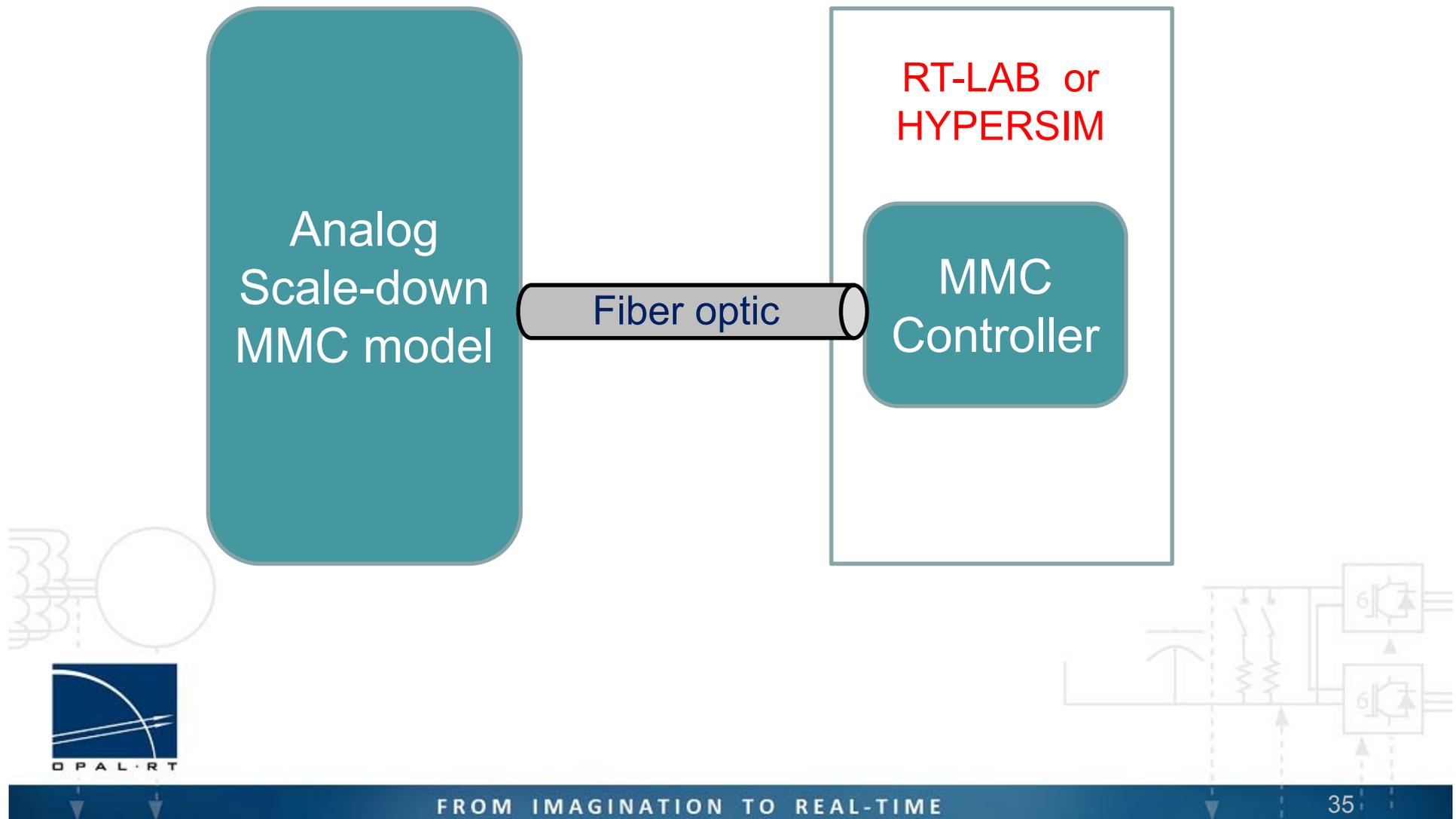
# Digital Simulating of MMC System



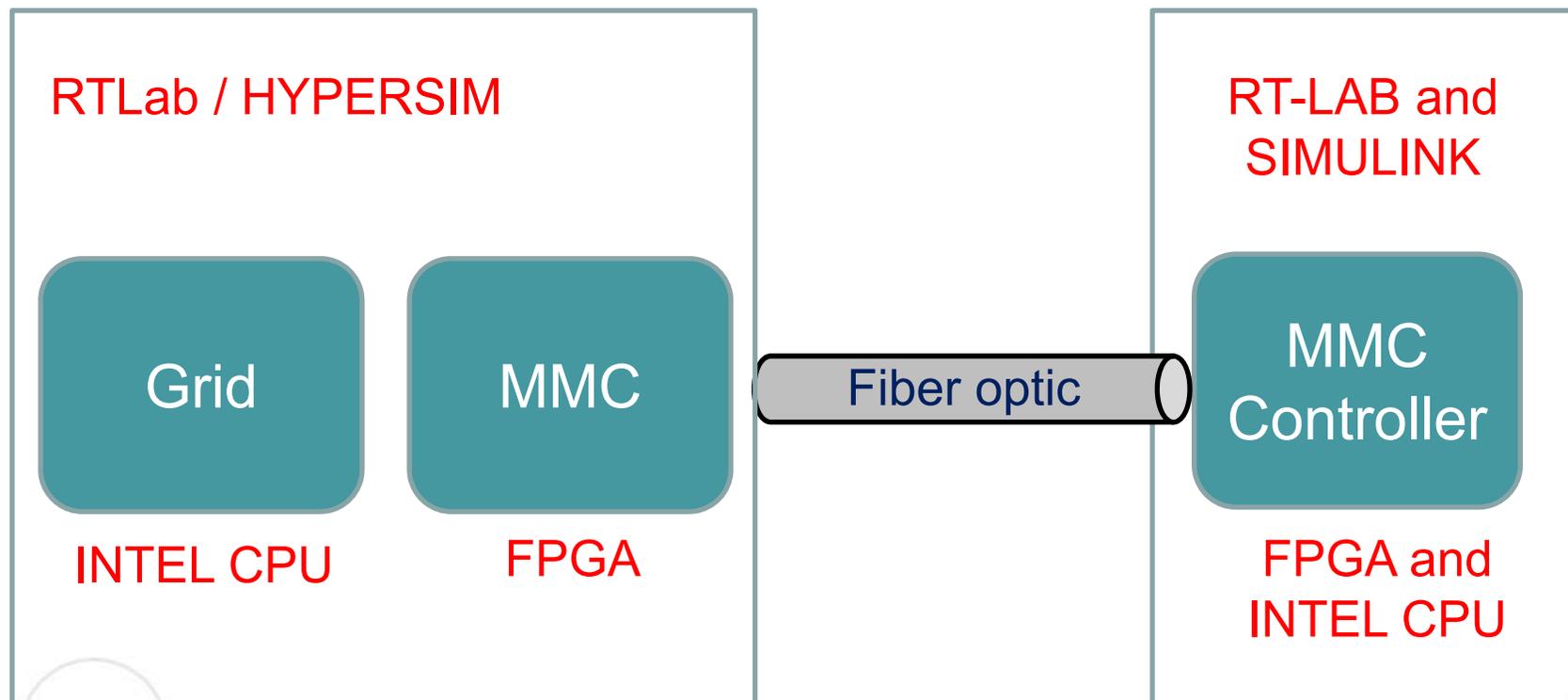
# HIL Testing of Actual MMC Controller



# MMC Rapid Control Prototyping (RCP)



# MMC RCP with Virtual MMC plant and AC grid



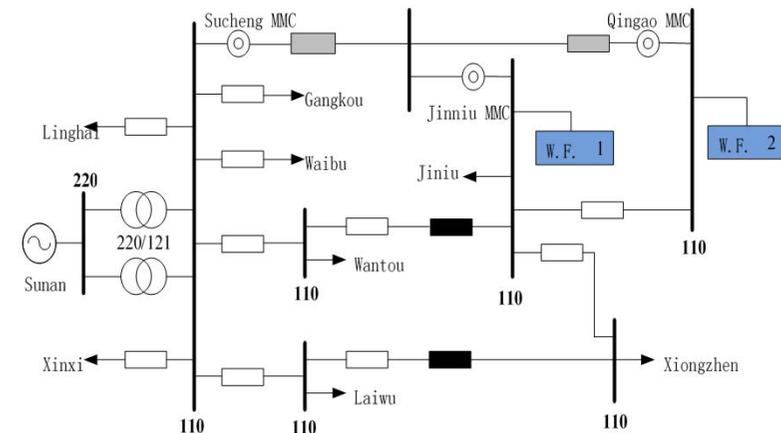
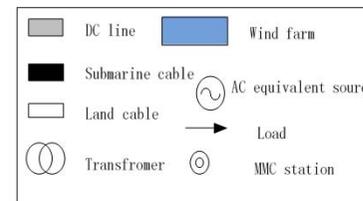
Very convenient setup for MMC controller development  
Fast interactivity – fast batch-mode optimization



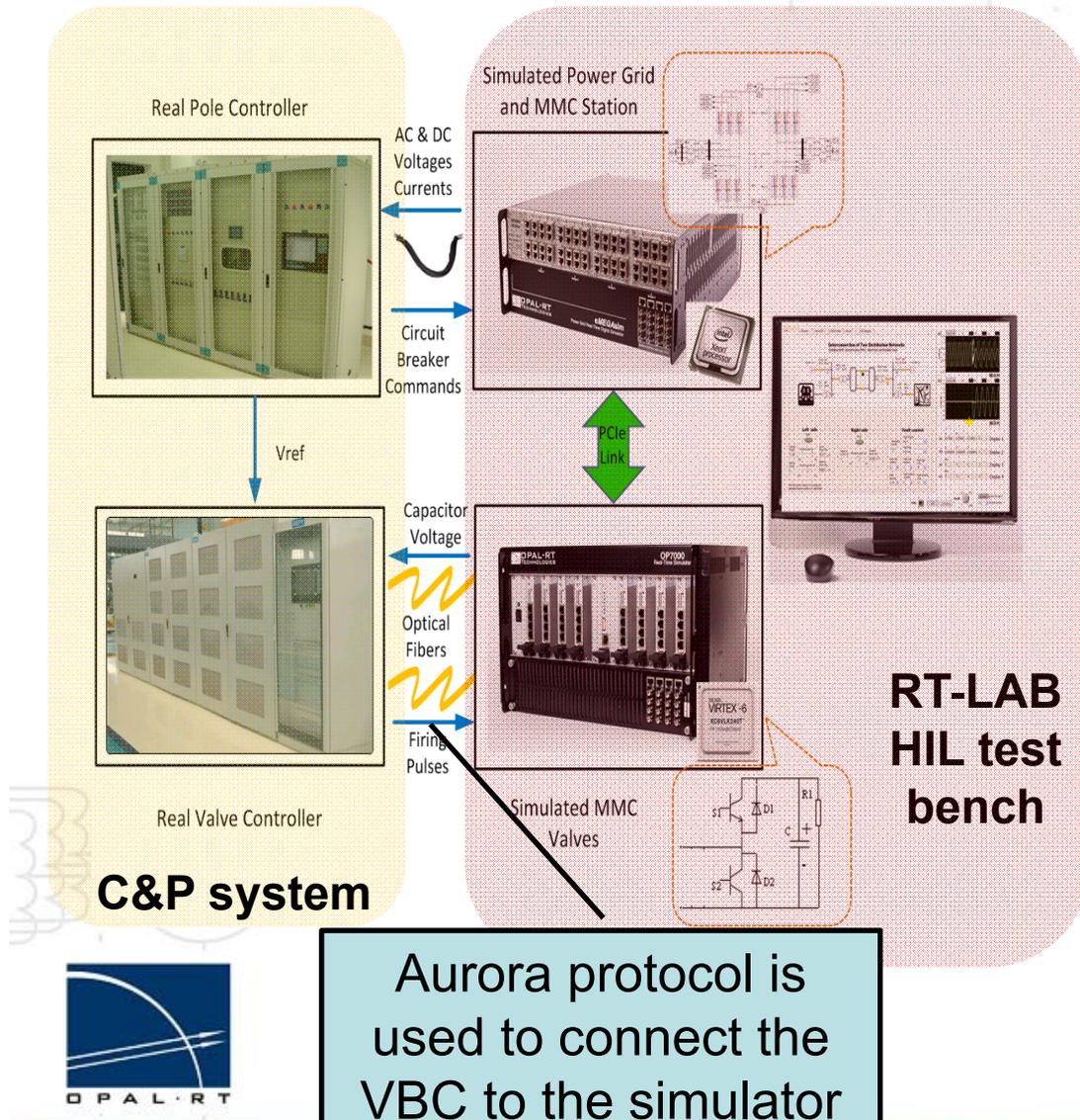
# System model of Nanao project

Parameters	Sucheng station	Jinniu station	Qingao station
Transformere connection	Yn/D11	Yn/D11	Yn/D11
Rated power (MVA)	240	120	63
Primary voltage (kV)	110	110	110
Secondary voltage (kV)	166	166	166
Primary impedance (pu) [R1,L1]	[0.0025 0.06 ]	[0.0025 0.06 ]	[0.0025 0.05 ]
Secondary impedance (pu) [R2,L2]	[0.0025 0.06 ]	[0.0025 0.06 ]	[0.0025 0.05 ]
Grounding resistance (kΩ)	5	5	5
MMC capacity(MVA)	200	100	50
Number of SMs in an arm	147	220	220
Number of redandant SMs	14	20	20
Rated SM voltage(kV)	2.4	1.6	1.6

## The three multi-terminal VSC HVDC project



# HIL testing system



Time Step	28 us
CPU #	6 (3 cpu for 3 Converters 1 cpu for ac grid 1 cpu for wind farm 1 cpu for data acquisition and logging)
FPGA #	3 Virtex-6
IO	32*3 AO 32*3 DI 32*3 DO

# Test matrix and sequence

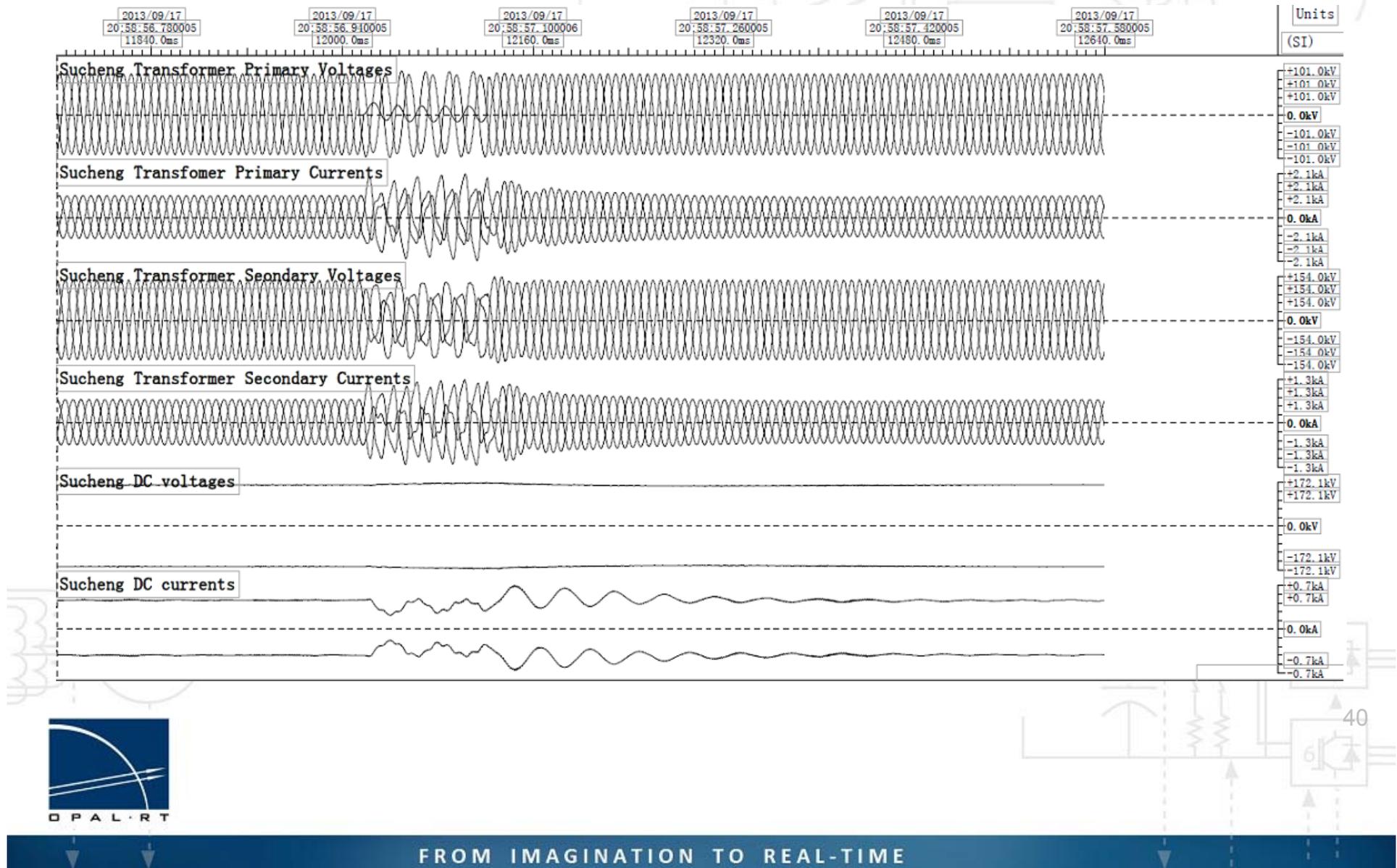
DPT	STATCOM	AC & HVDC	Pure DC Operation
FPT	STATCOM	AC & HVDC	Pure DC Operation
R&D	STATCOM operation	AC & HVDC Operation	Pure DC Operation
<ul style="list-style-type: none"> <li>• Auto Start sequence</li> <li>• Power step command</li> <li>• PCP redundancy</li> <li>• Internal communication failure</li> <li>• AC faults</li> <li>• DC faults</li> <li>• Valve faults</li> </ul>	<ul style="list-style-type: none"> <li>• Auto Start sequence</li> <li>• Power step command</li> <li>• PCP redundancy</li> <li>• Internal communication failure</li> <li>• AC faults</li> <li>• DC faults</li> <li>• Valve faults</li> </ul>	<ul style="list-style-type: none"> <li>• Auto Start sequence</li> <li>• Power step command</li> <li>• PCP redundancy</li> <li>• Operation with and without substation communication</li> <li>• AC faults</li> <li>• DC faults</li> <li>• Valve faults</li> </ul>	<ul style="list-style-type: none"> <li>• Auto Start sequence</li> <li>• Power step command</li> <li>• PCP redundancy</li> <li>• Operation with and without substation communication</li> <li>• AC faults</li> <li>• DC faults</li> <li>• Valve faults</li> </ul>

The same test scenarios are repeated at different stage of production.

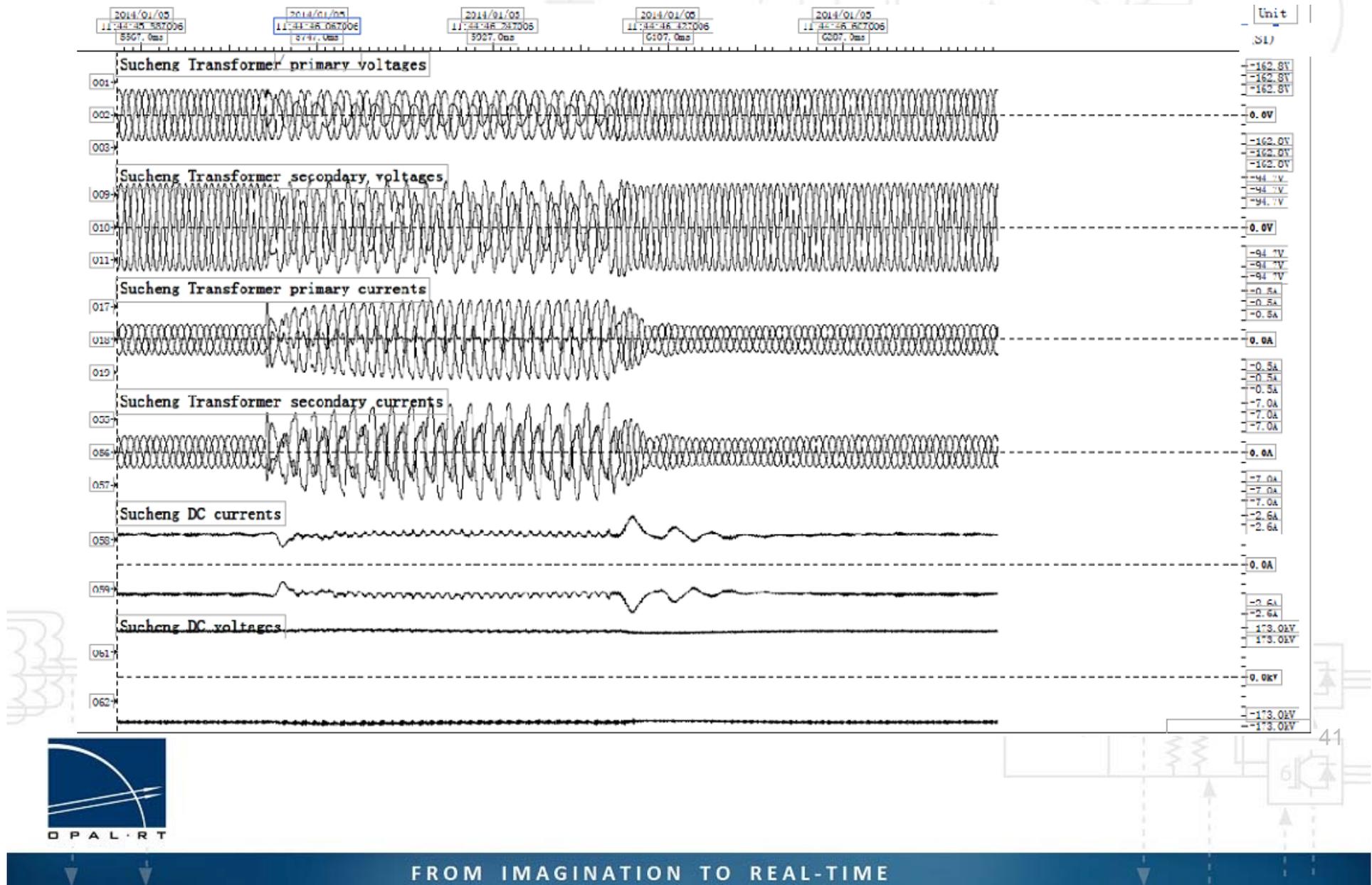
\* FPT: Functional performance test; DPT: Dynamic performance test



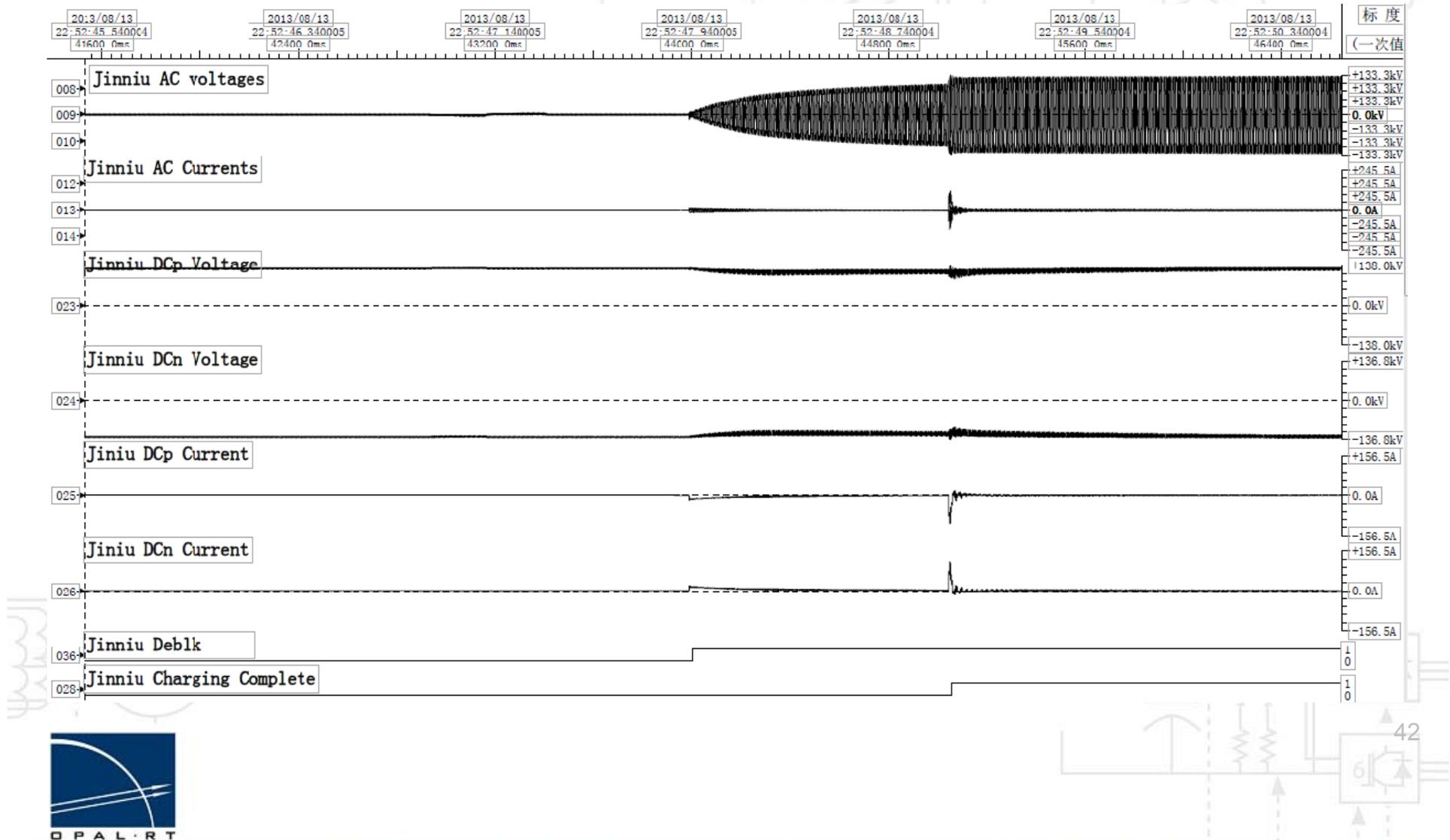
# HIL Test results (F1) - Nanao project



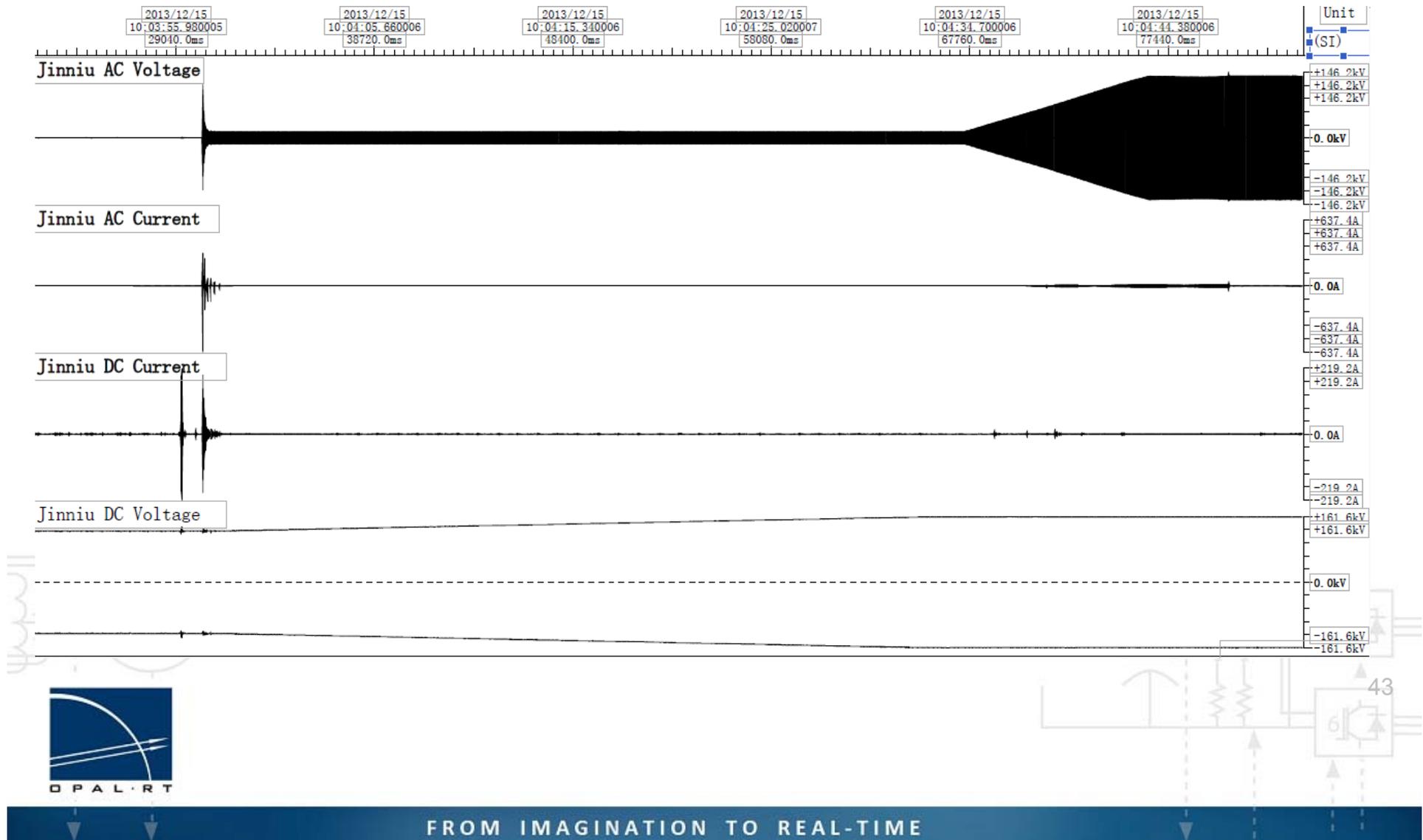
# Field Test results (F1) - Nanao project



# HIL results (DC charging) – Nanao project

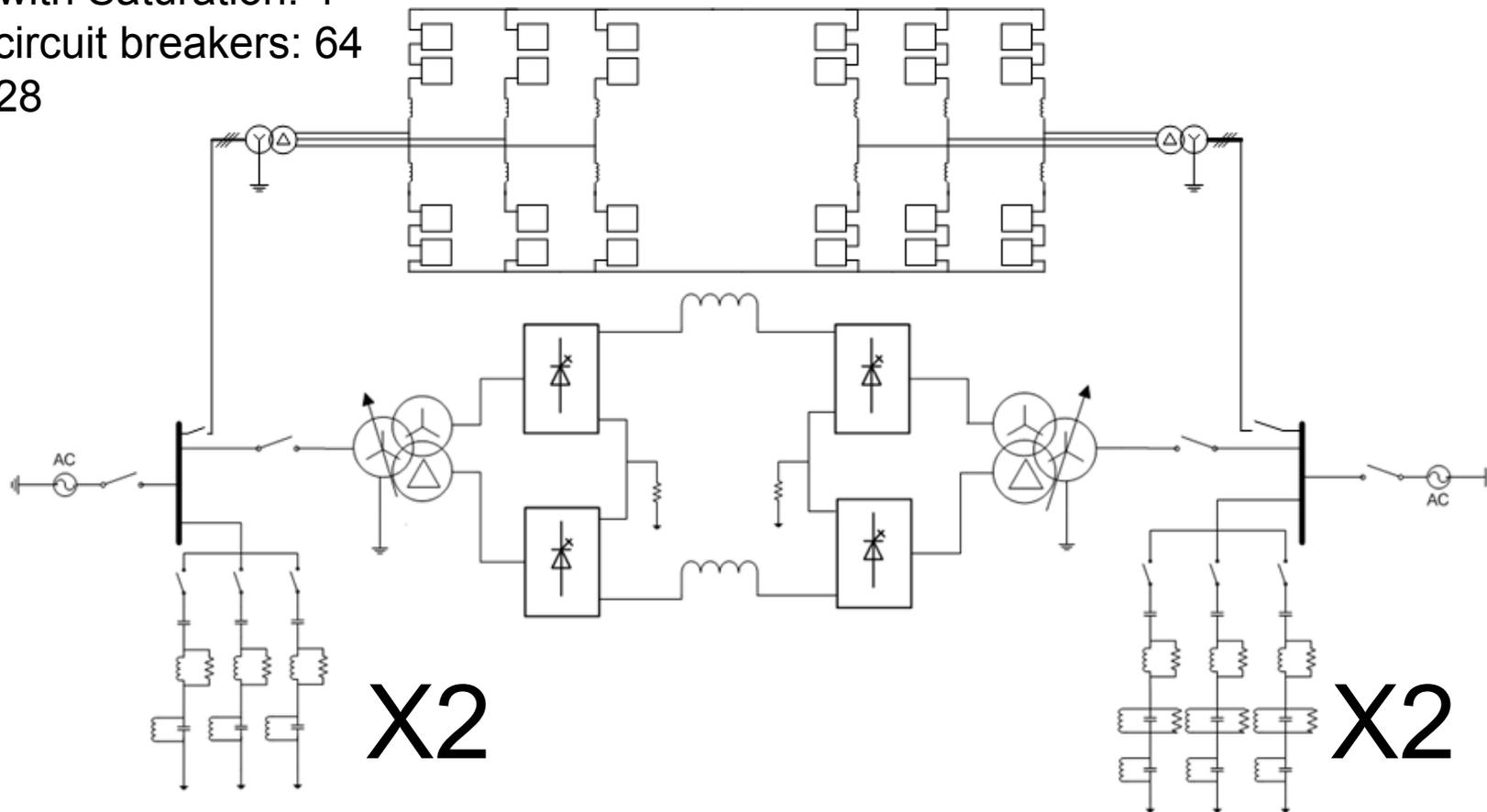


# Field Test Results (DC charging) – Nanao project

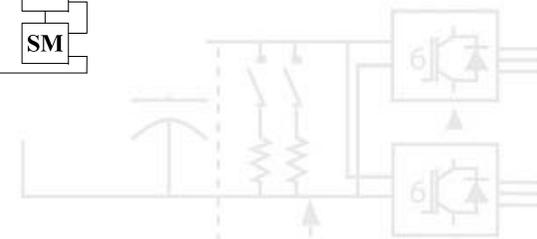
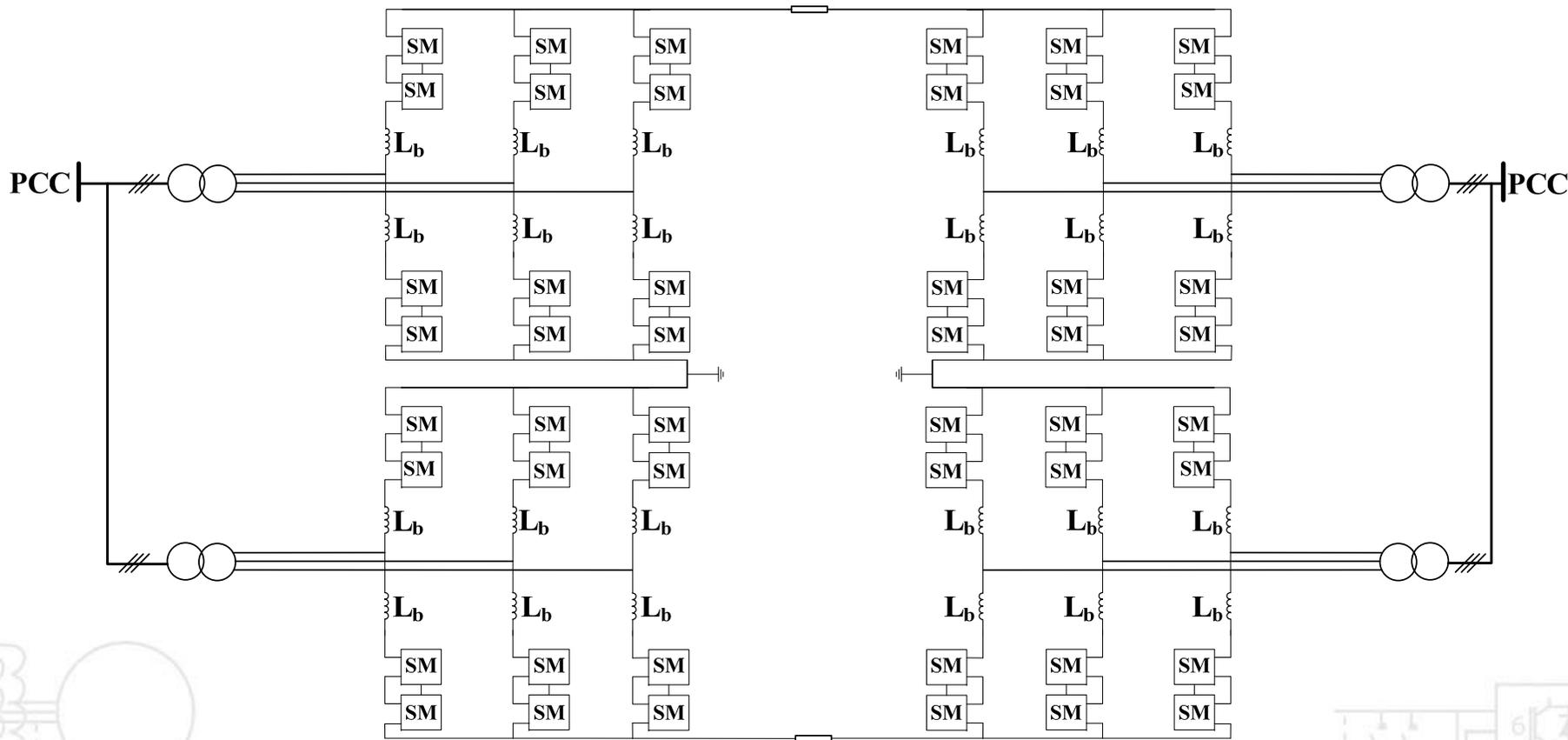


# Luoping (Yunnan Project)

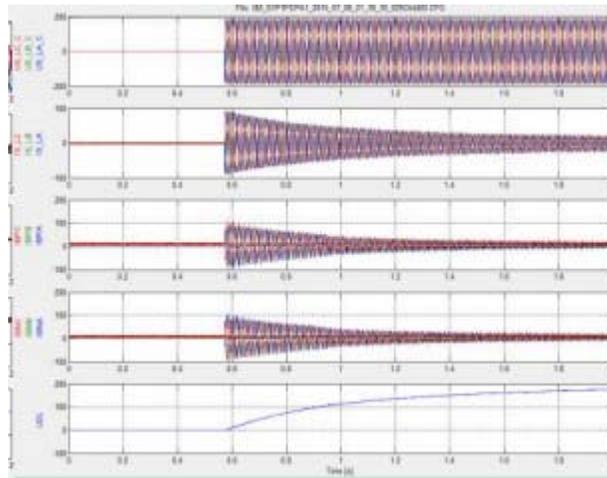
- ❖ MMC: 2 converters with 400 half-bridge submodules per valve (or 800 per arm)
- ❖ LCC: 2 converters with 12 thyristor each
- ❖ Passive filters with circuit breakers: 6 at each terminal
- ❖ OLTC with Saturation: 4
- ❖ Other circuit breakers: 64
- ❖ MOV: 28



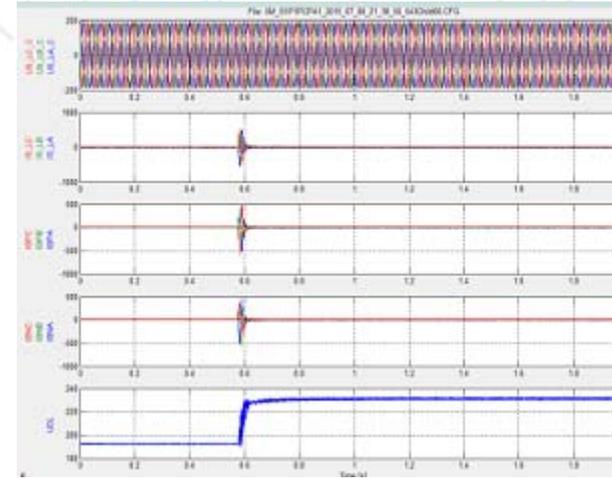
# Xiamen MMC-based Bi-pole HVDC



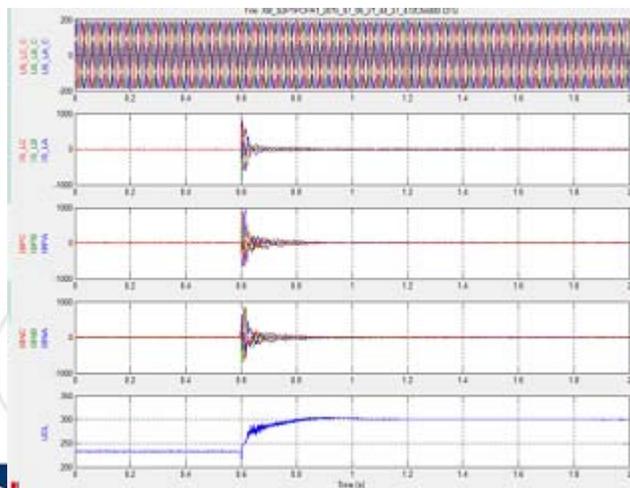
# HIL results (start-up) – Xiamen project



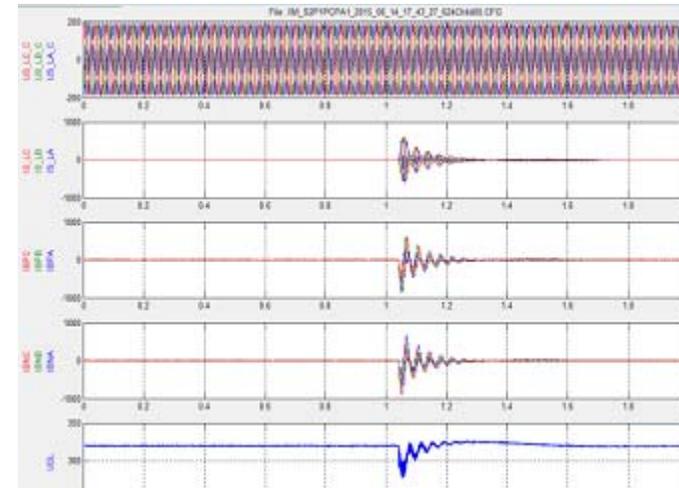
Closing Ac breaker



Closing charging resistor bypass breaker



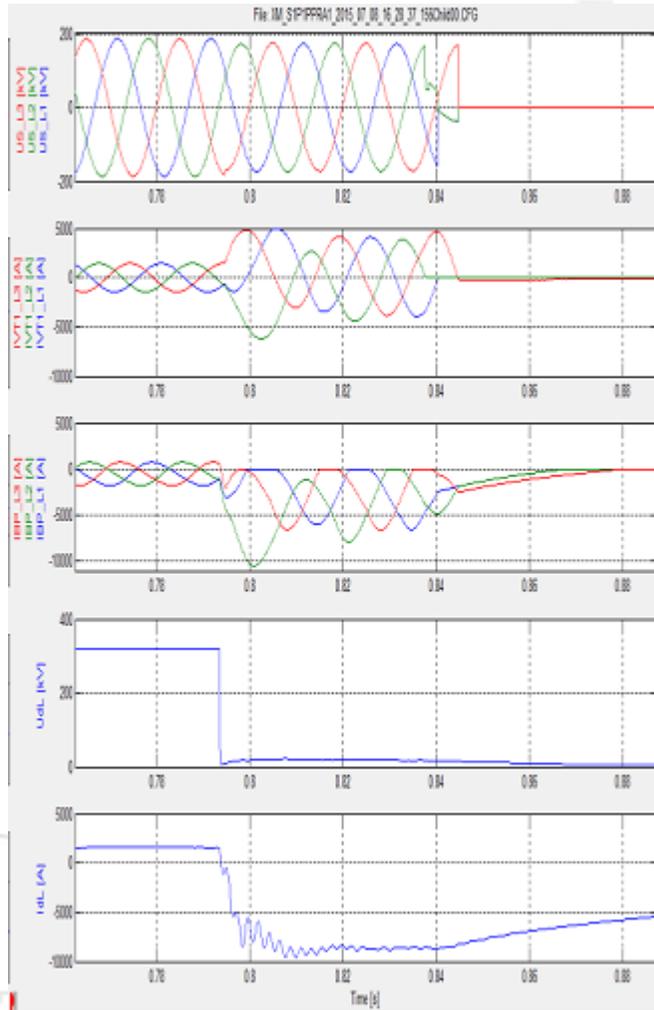
Pulse enable at station controlling Vdc



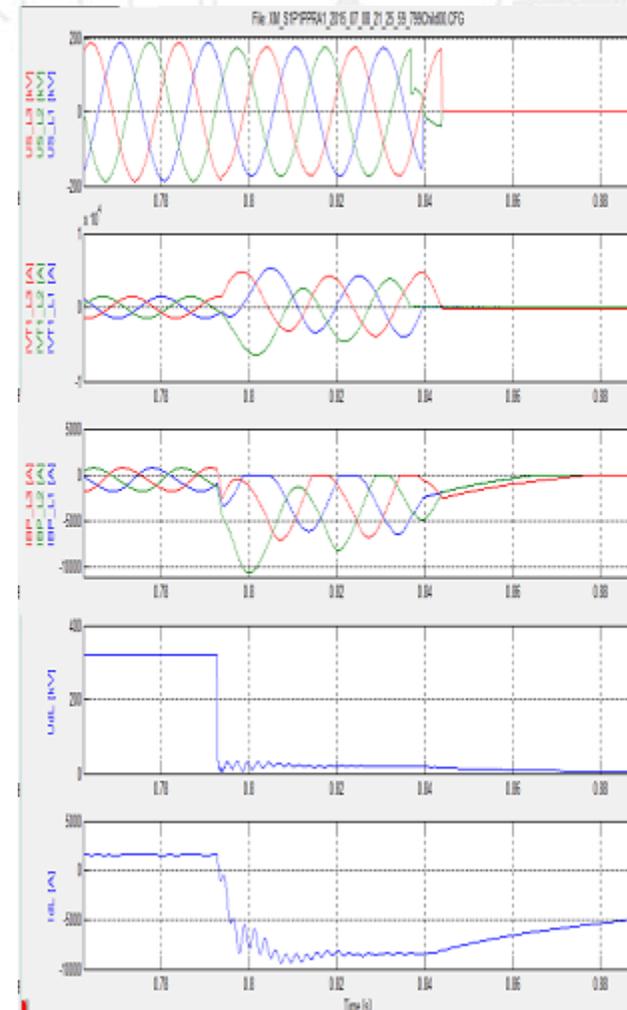
Pulse enable at station controlling active power



# HIL results (faults) – Xiamen project



Positive dc pole to ground fault



Positive-to-negative dc fault



# MMC Lab-scale test bench for RCP

Cabinet (Front view)



40U Standard Cabinet  
(1U = 1.75 inch)

## OP1200 - Rapid control prototyping for Power Electronics Converters Modular, flexible, configurable

Configurable for different type of converter, topology, number of level (11, 21, 31...), DC Voltage (400V, 700V...), frequency (50Hz, 60Hz) and the output power (6kW, 10kW, 20kW...)

Specifications for a 3-Phases MMC Test Bench with 6kW 400V 11-Level for a total of 60 H-bridge cells in one cabinet

Technical specifications	Value (6 Arm / 11 levels)
DC Maximum Voltage per 10 cell	400 V
DC Maximum Current by arm, I phase	15 Arms (1800VA)
Maximum Output Power	6 KW
Max AC Voltage for each phase (with index modulation at 0.9)	120/208 V 3ph
Max AC RMS current at fundamental frequency	16.7 A
MOSFET Switching Frequency	0-10 kHz
Number of levels	11
Maximum Cell Voltage	40 V
Cell Capacitor	6 mF
Arm inductor	1.75 mH

# MMC Lab-scale test bench for RCP

Example for a 3-Phases MMC Test Bench with 10 cells per arm, for a total of 60 H-bridge cells

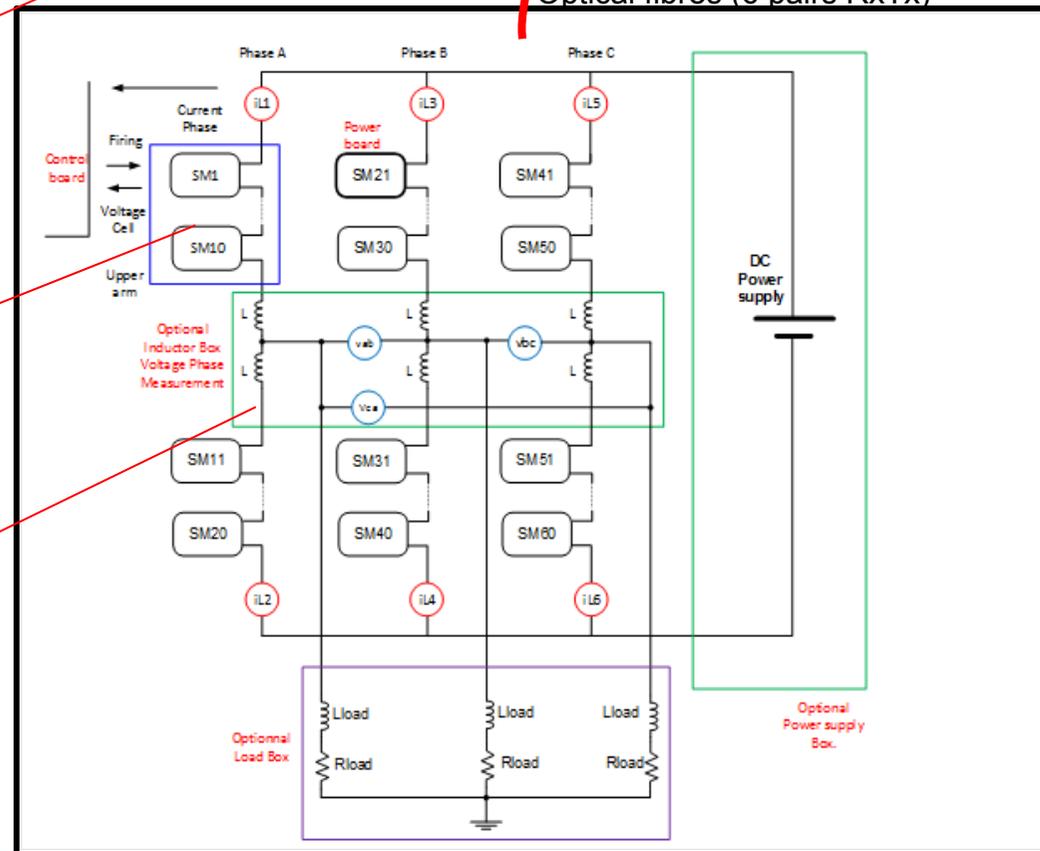


OP4510 Real-Time Simulator  
Intel Xeon Processor and Xilinx FPGA

Cabinet (Front view)



40U Standard Cabinet (1U = 1.75 inch)



Optical fibres (6 pairs RxTx)

# OP1200 OPAL-RT Lab-Scale MMC Test Bench

The **OP1200**, OPAL-RT Lab-Scale MMC Test Bench, includes:



**OP1200** – Fully integrated MMC Test Bench

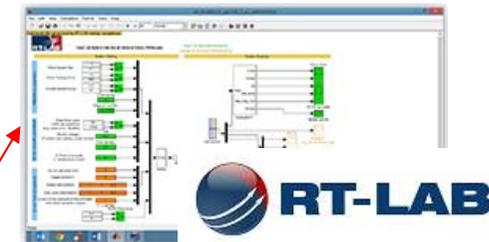
**RT-LAB MATLAB/Simulink® and XILINX System Generator**  
FPGA IP and SIMULINK demo controller for AC-DC 3-phase MMC, 11 level

**OP4510** - Real-time Simulator, Intel Xeon Processor and Xilinx FPGA with basic MMC controller Simulink and FPGA IP

**OP1210** - 10 H-bridge cells MMC Converter 2U module with OP1211 control board and 10 OP1212 cell modules

**OP1211** – Valve Based Electronic control board

**OP1212** - IGBT H-bridge Capacitor Switch Sub-Module



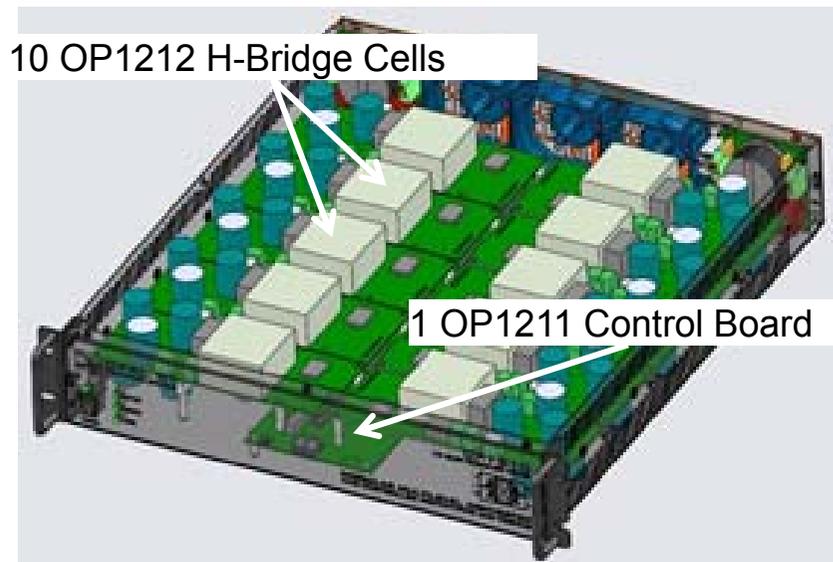
# OP1210 - 10 H-bridge cells MMC Converter Specifications

Opal-RT provides a lab **Modular Multilevel Converter (OP1210)** 2U module  
Scalable up to 10 H-bridge cells. The OP1210 is designed for 2KW (Rail or Shelves)

Technical specifications	Values
Power Supply	48V
Total Number of H-Bridge Cells	10
Number of power output connectors	2
Max DC Voltage per cell	40 VDC
Max RMS current per arm	15 A
Serial Communication (Tx/Rx Fiber Optic)	50/10 Mbps
Switch status refresh rate	500 ns
ADC sample rate (Cell voltage and current)	50 kHz
Desktop/Rack (Rail or Shelves)	Height 2U Depth 20"
Weight	10Kg



10 OP1212 H-Bridge Cells

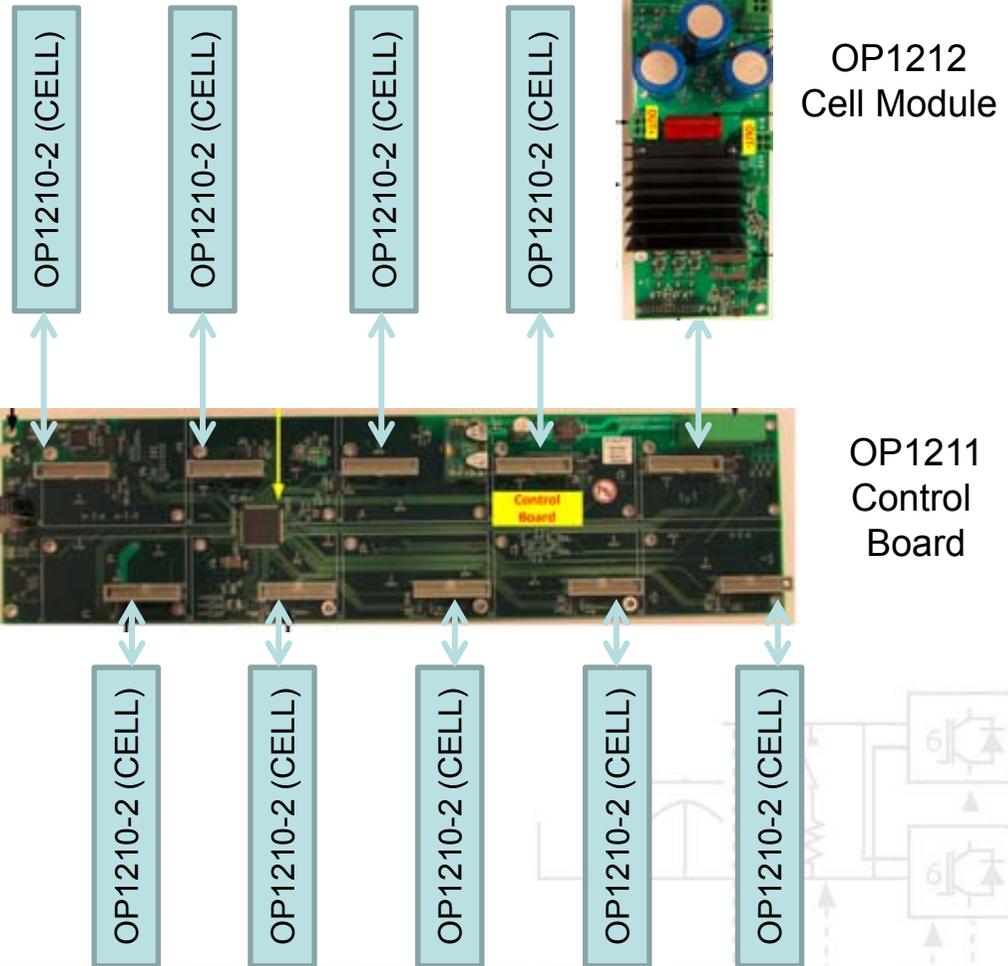


# OP1210 - 10 H-bridge cells MMC Converter Module Bloc Diagram

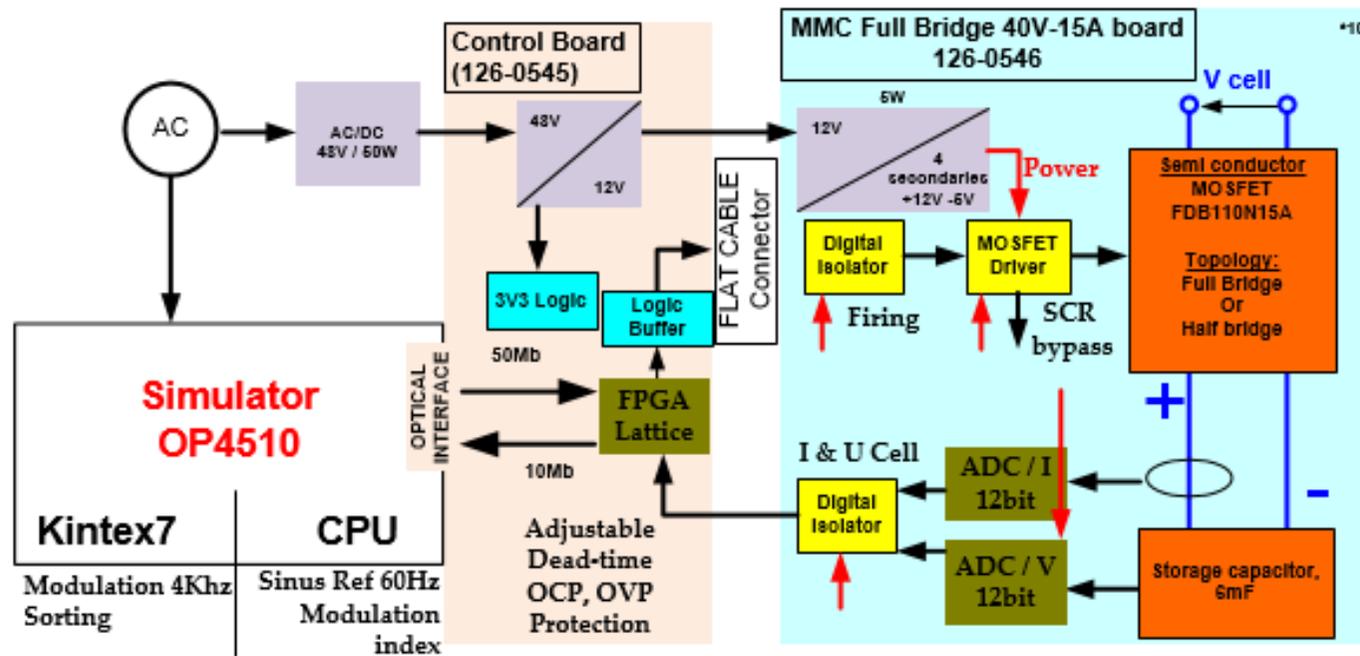
## OP1210: 10-cell Module



**OP4510** - Real-time Simulator  
Intel Xeon Processor (4 cores)  
Xilinx FPGA (Kintex7 325T)



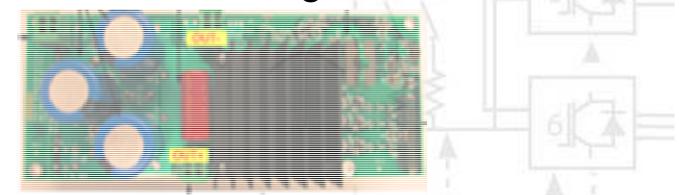
# OP1210 - 10 H-bridge cells MMC Converter Module Detailed Block Diagram



OP1211 Control board for 10 cells



OP1212 H-Bridge Cell



# Summary

- MMC C&P systems is very complex, making complete integration test before commissioning is extremely important
- HIL complements off-line simulation tools:
  - To increase simulation speed to meet tight development schedule
  - To increase testing coverage by doing more tests in less time
  - To increase fidelity by interfacing with actual hardware
  - To perform large integration tests with several controllers
  - All of the above are to reach the goal of better MMC C&P system quality by thorough validation of real life situation
- Multi-levels converter with multi-terminals require continues improving of the HIL tools



# Summary

Challenges	OPAL-RT Solutions
Very small time step for SM	250 ns or 500 ns
Small time step for AC grid, arm inductors and transformer	20 to 60 micros using ARTEMIS-SSN or HYPERSIM nodal solver
Very small time step for arm inductor and transformer models	500 ns to 1 us using eHS FPGA nodal solver (Q4 2014)
Large number of SM per converter	1500 to 6000 cells per FPGA
Large number of terminal for HVDC grids	Use several FPGA boards (systems with up to 10 FPGA have been delivered)
Connection to controller with fast rate and small latency	Aurora or Gigabit Ethernet 1 to 5 us update depending on number of optical fiber links and number of cells
Accuracy for non-linear elements, e.g. MOV for fault simulation and other large disturbances	Iterative solver
Tested reliability	Several projects



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2. O. Venjakob, S. Kubera, R. Hibberts-Caswell, P.A. Forsyth, T.L. Maguire, "Setup and Performance of the Real-Time Simulator used for Hardware-in-Loop-Tests of a VSC-Based HVDC scheme for Offshore Applications", Proceedings of International Conference on Power Systems Transients (IPST'13), Vancouver, Canada, July 18-20, 2013.
3. H. W. Dommel, "Digital computation of electromagnetic transients in single and multi-phase networks," IEEE Trans. Power App. Syst., vol. PAS-88, no. 4, pp. 388–399, Apr. 1969.
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7. H. Saad, C. Dufour, J. Mahseredjian, S. Denetière, S. Nguéfeu, "Real Time simulation of MMCs using the Combined State-Space Nodal Approach," Proceedings of International Conference on Power Systems Transients (IPST'13), Vancouver, Canada, July 18-20, 2013.
8. T. L. Maguire, B. Warkentin, Y. Chen, and J. Hasler, "Efficient Techniques for Real Time Simulation of MMC System", Proceedings of International Conference on Power Systems Transients (IPST'13), Vancouver, Canada, July 18-20, 2013.
9. W. Li; J. Belanger, "An Equivalent Circuit Method for Modelling and Simulation of Modular Multilevel Converter in Real-time HIL Test Bench," IEEE Transactions on Power Delivery, 2016





Thanks.

