SIGNAL INTEGRITY AND POWER INTEGRITY:

CHALLENGES AND TEST SOLUTIONS

ROHDE&SCHWARZ

Make ideas real

INDUSTRY TRENDS AND TECHNICAL CHALLENGES
EVOLUTION OF KEY TECHNOLOGIES FOR DATA CENTERS

PCIe: Processing, Storage

PCIe Spec.	Raw BW (per lane)	Modulation NRZ / PAM	Symbol Rate (per lane)
…			
PCIe 4.0: for 16.0 GT/s	16.0 Gbps	NRZ	16.0 GBd
PCIe 5.0 for 32.0 GT/s	32.0 Gbps	NRZ	32.0 GBd
PCIe 6.0 for 64 GT/s	64.0 Gbps	PAM4	32.0 GBd
PCIe 7.0 for 128 GT/s	…	…	…

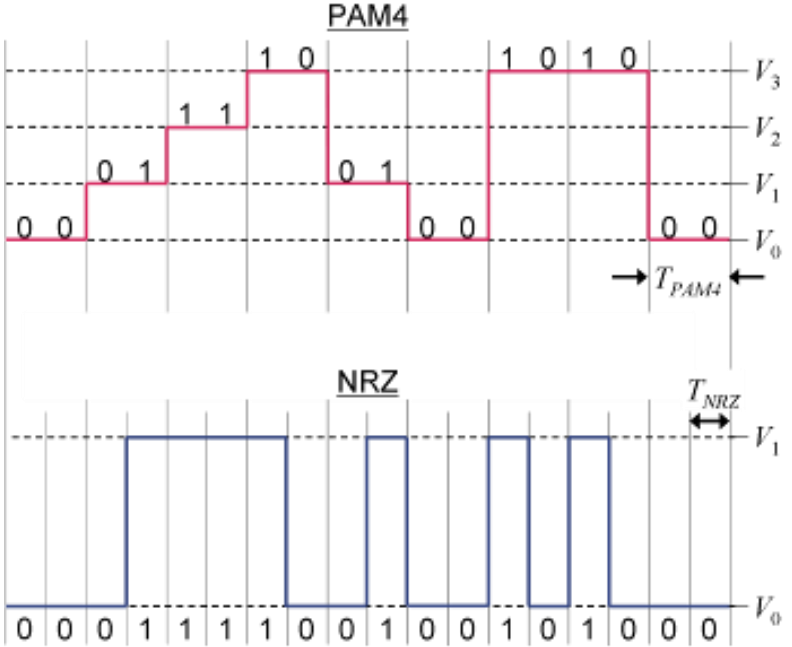
used cable formats: x1, x2, x4, x8, x16

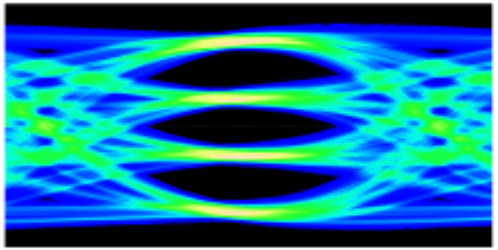
IEEE 802.3: Datacom

IEEE Spec.	Raw BW (per lane)	Modulation NRZ / PAM	Symbol Rate (per lane)
…	…		
802.3bj/by	25.78125 Gb/s	NRZ	25.78125 GBd
802.3cd	53.125 Gb/s	PAM4	26.5625 GBd
802.3ck	106.25 Gb/s	PAM4	53.125 GBd
802.3dj	…	…	…

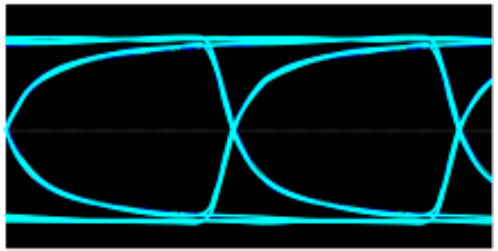
used cable formats: CR1, CR2, CR4, CR8, CR16

GENERAL SIGNAL INTEGRITY CHALLENGES: CROSSTALK IN SYSTEMS WITH PAM 4 VS NRZ





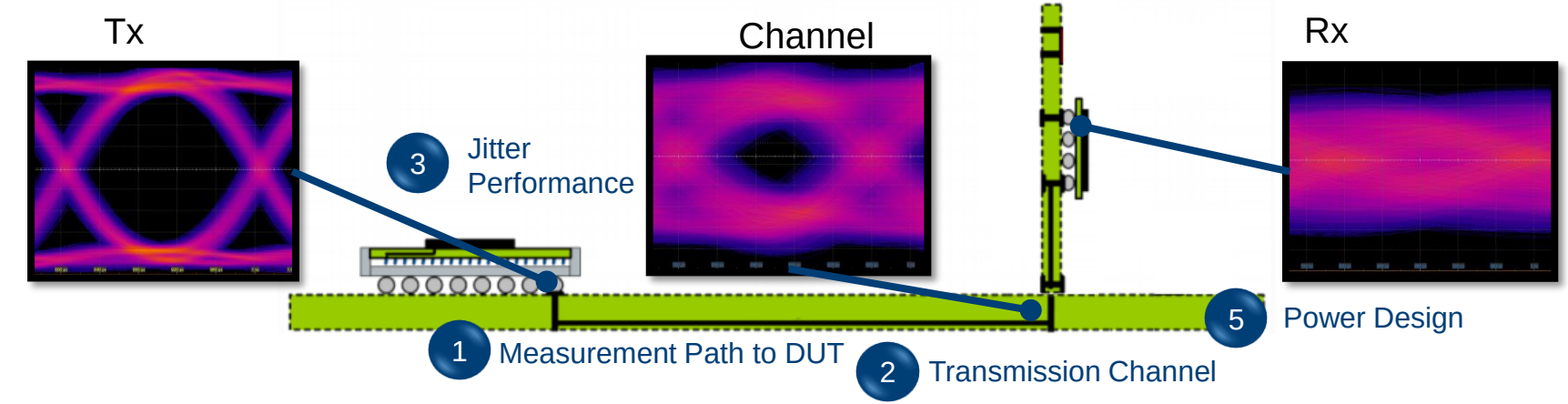
$$BW_{PAM4} = ½\ BW_{NRZ}$$

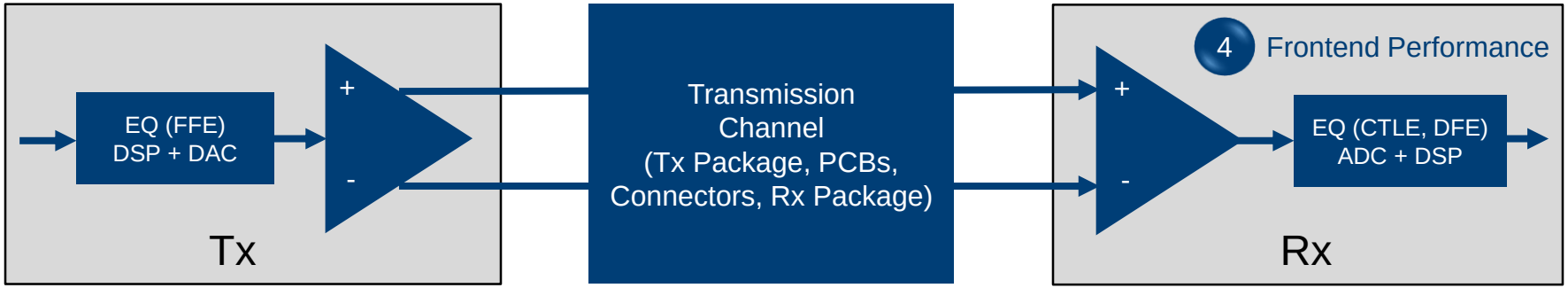


eye height for PAM4 is 1/3 of eye height for NRZ: 20 log (1/3) = -9.5 dB

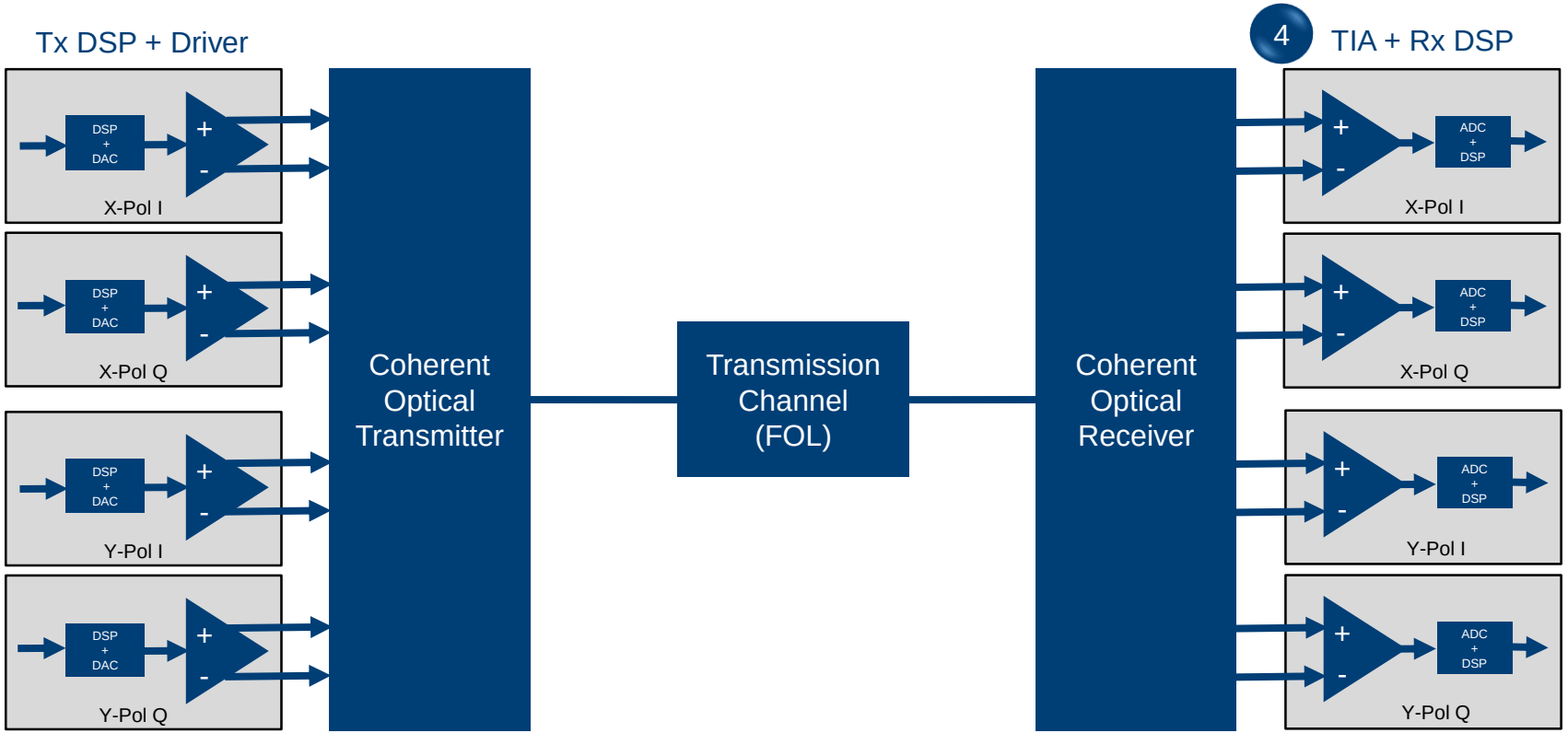
→ higher sensitivity to noise and crosstalk

TRANSMISSION CHANNEL AND VALIDATION CHALLENGES ELECTRICAL INTERFACES



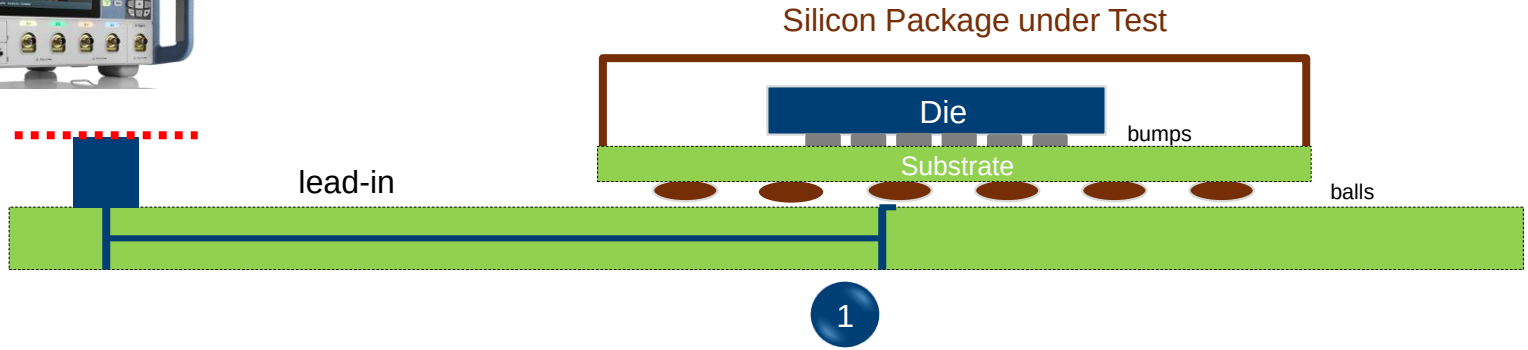


TRANSMISSION CHANNEL AND VALIDATION CHALLENGES OPTICAL INTERFACES



Measurent Plane:

- Oscilloscope (Tx)
- BERT / AWG (Rx)
- VNA (RL)



CHALLENGE 1: CHARACTERIZING AND DE-EMBEDDING THE MEASUREMENT PATH TO THE SOC

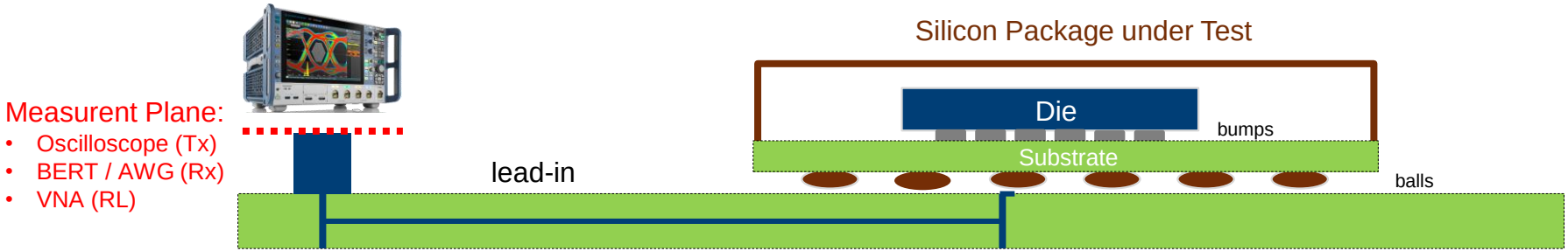
CHALLENGE 1: CHARACTERIZING AND DE-EMBEDDING THE MEASUREMENT PATH TO THE SOC

Challenge:

- measurement parameters required at BGA interface
- measurememt path to DUT needs to be characterized for de-embedding in
  - Oscilloscope: Tx validation
  - BERT / AWG: Rx validation
  - VNA: RL measurement

Solution:

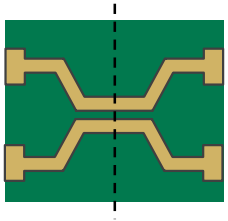
- test fixture characterization and de-embedding
- DC extrapolation (for scopes, BERTs / AWGs)



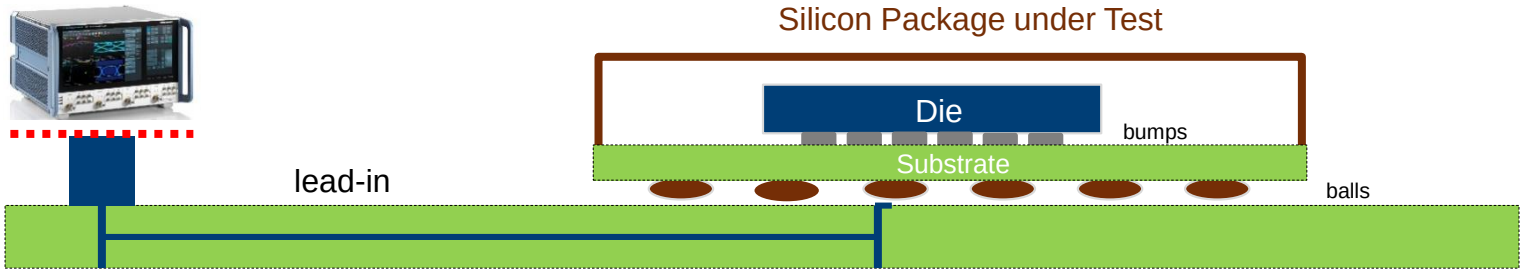
CHALLENGE 1: CHARACTERIZING AND DE-EMBEDDING THE MEASUREMENT PATH TO THE SOC

Method 1: Measurement with SOC

- step 1: 4-port measurement of reference structure (i.e. 2x-Thru)



- step 2: 2-port measurement of total structure

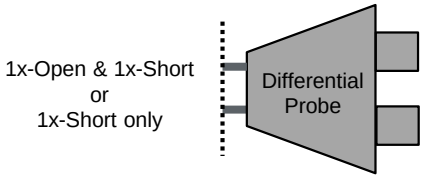


- step 3: S-parameter model of lead-in incl. DC extrapolation

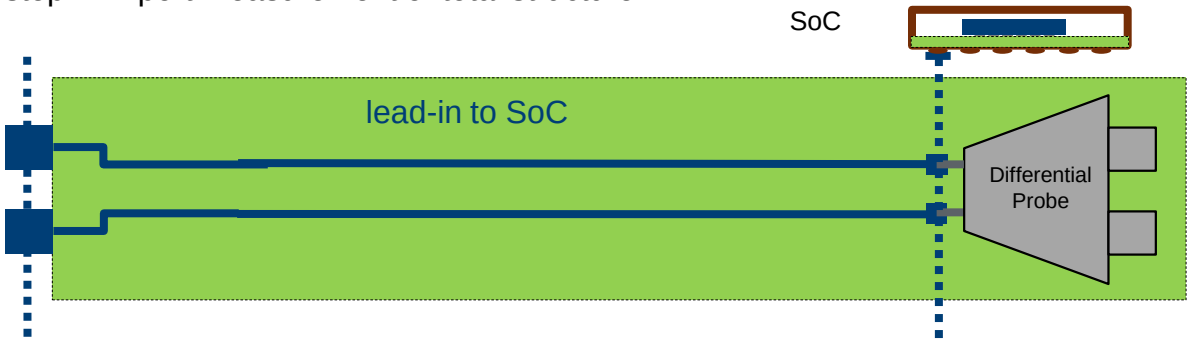
CHALLENGE 1: CHARACTERIZING AND DE-EMBEDDING THE MEASUREMENT PATH TO THE SOC

Method 2: Measurement without SOC

- step 1: 2-port measurement of reference structure (i.e. 1x-Open & 1x-Short)



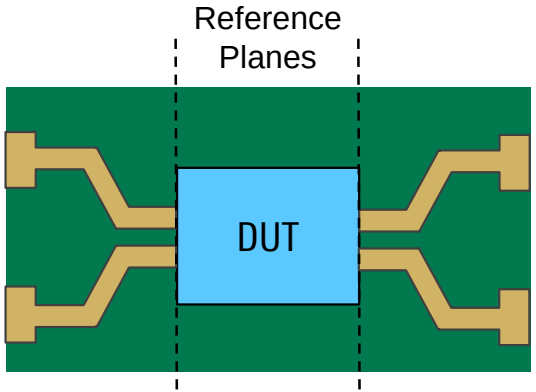
- step 2: 4-port measurement of total structure



- step 3: S-parameter model of lead-in incl. DC extrapolation

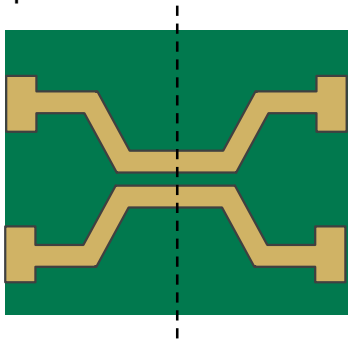
ACCURATE TEST FIXTURE MODELING AND DE-EMBEDDING: HOW IT WORKS – IMPEDANCE CORRECTED DE-EMBEDDING

Total Structure
Fixture – DUT – Fixture



with

2x-Thru Coupon
Replica of Lead-in / Lead-out



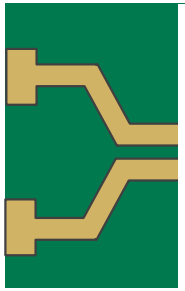
Traditional 2x-Thru de-embedding:
fixture models were only derived from 2x-Thru Coupon (replicas)

But:
replicas typically have different impedance profiles than actual lead-ins / lead-outs!

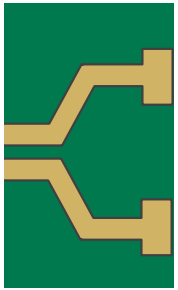
Therefore:
use modern de-embedding with impedance correction

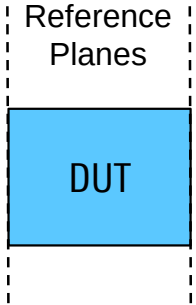
Algorithm

Fixture 1 Model:
Lead-in traces



Fixture 2 Model:
Lead-out traces

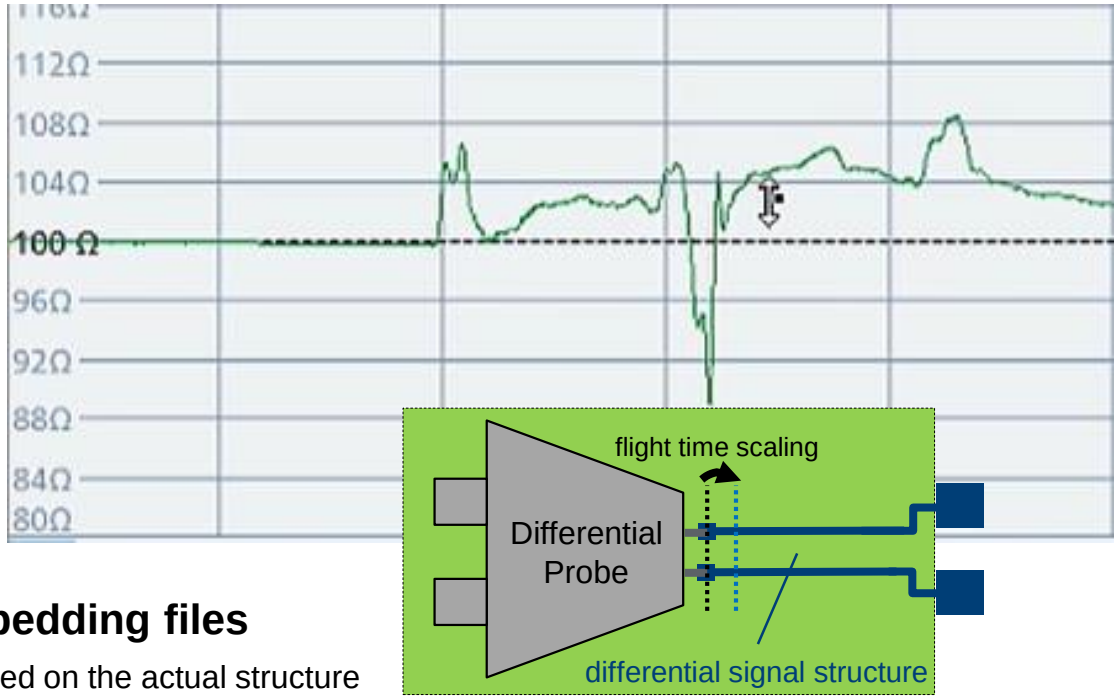




ACCURATELY MODELLING AND DE-EMBEDDING OF DIFFERENTIAL PROBES: HOW FAR TO DE-EMBED?

How far do we need to de-embed?

- discontinuity at the probe tips is **not** part of the differential signal structure
- de-embedding has to be done past this discontinuity and slightly into the differential signal structure
- impedance corrected de-embedding to correctly model the probe and contact point discontinuity as it is on the board.



Limitation of factory-made de-embedding files

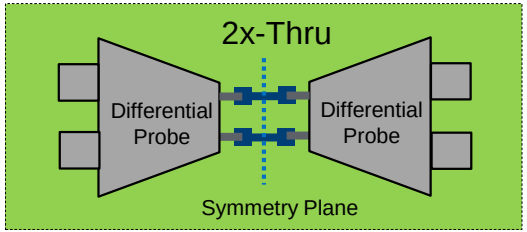
- recommendation to characterize and de-embed on the actual structure

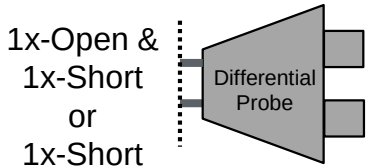
ACCURATELY MODELLING AND DE-EMBEDDING OF DIFFERENTIAL PROBES: CONCLUSION

Workflow of Impedance Corrected De-embedding:

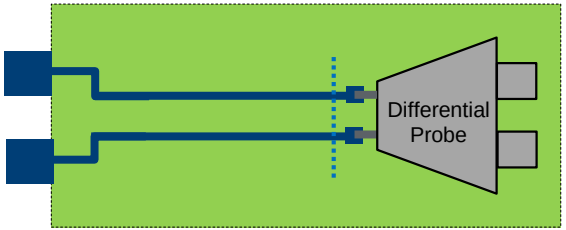
- calibration up to the coaxial interface of the VNA setup
- characterization and de-embedding of the probe:
  - total structure
  - de-embedding reference structures:
    - 2x-Thru or
    - 1x-Open & 1x-Short or
      1x-Short only
      with flight time scaling
      (move past discontinuity
      of probe contact point)
  - impedance correction required to correctly model probe contact discontinuity and shift reference plane into actual signal structure

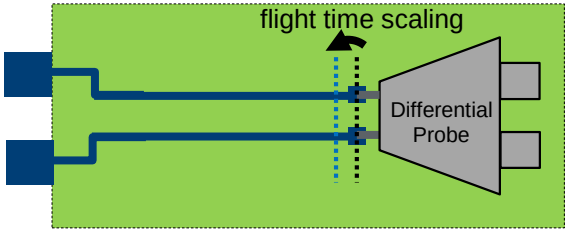
Reference Structure
(Coupon)





Total Structure
Fixture – DUT – Fixture

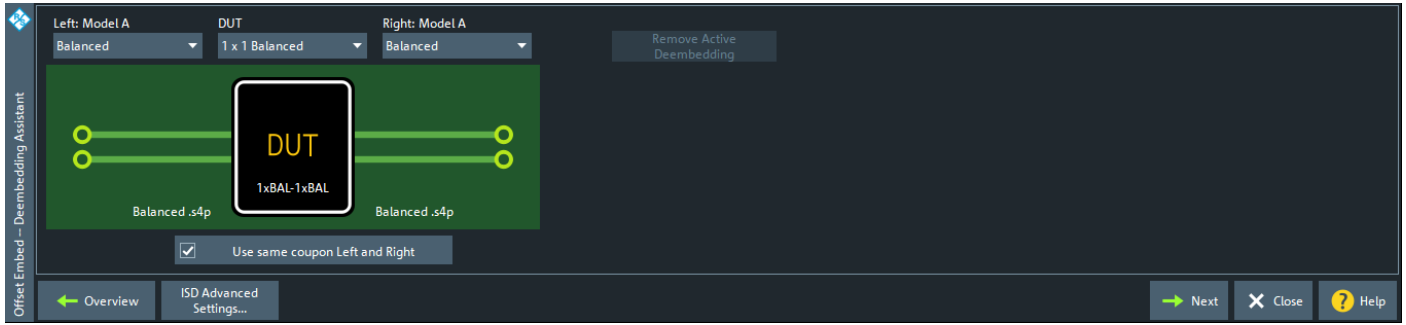




R&S DE-EMBEDDING ASSISTANT: ZNA, ZNB / ZNBT WORKFLOW WITH IMPEDANCE CORRECTION

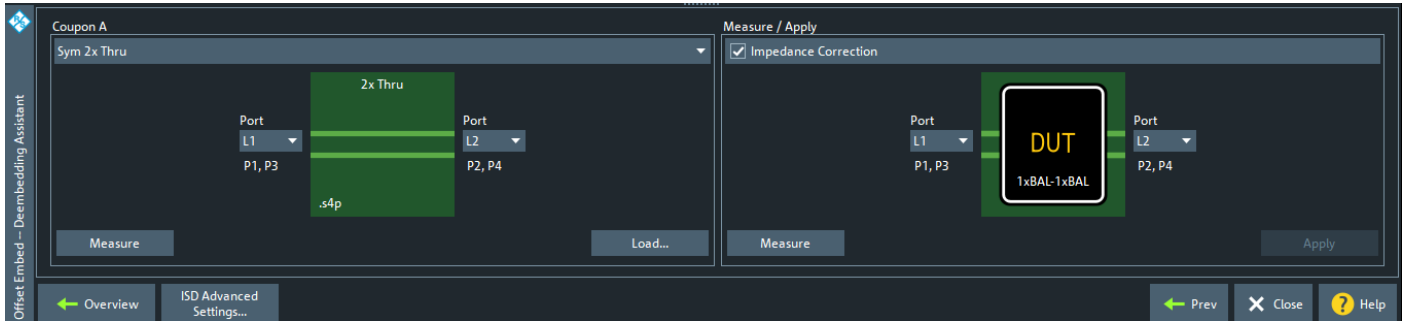
R&S De-embedding Assistant with Impedance Correction: Example ZNx-K220

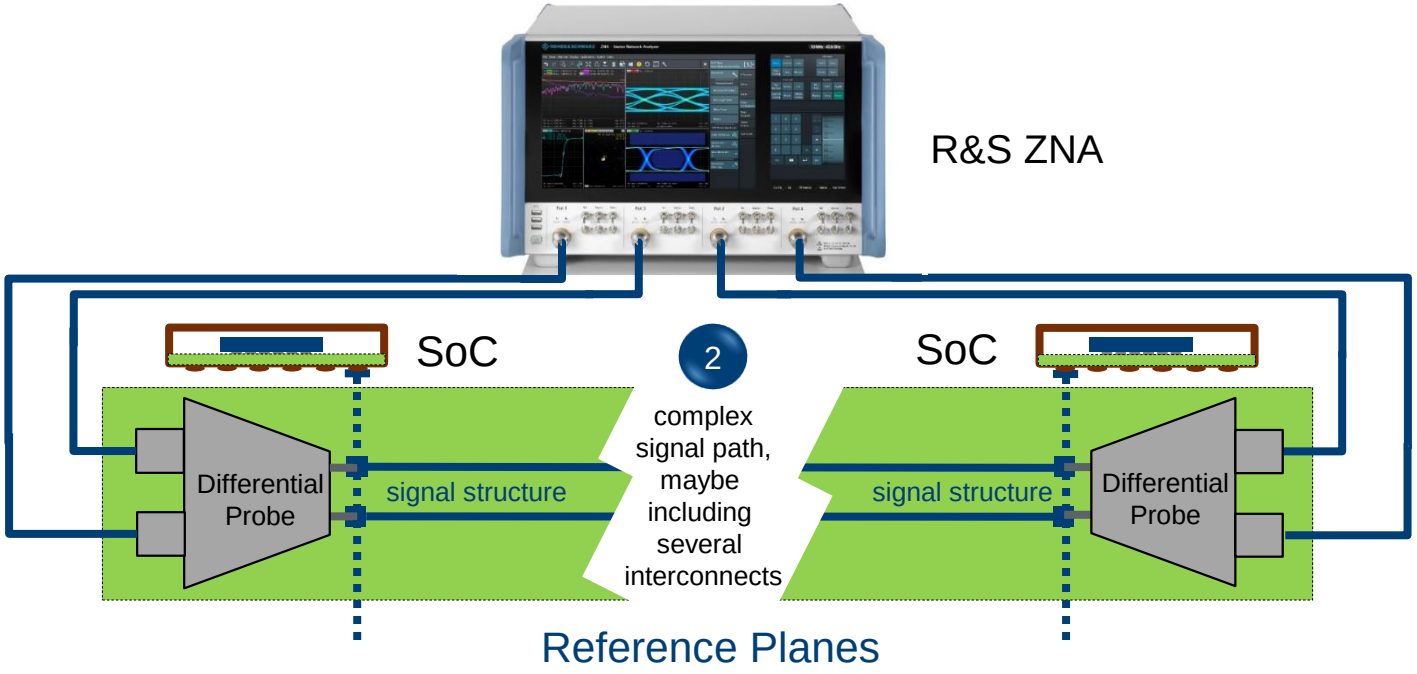
Step 1:
select topology
- DUT
- lead-in
- lead-out



Step 2:
measurements
- coupon(s)
- total structure

Step 3:
apply



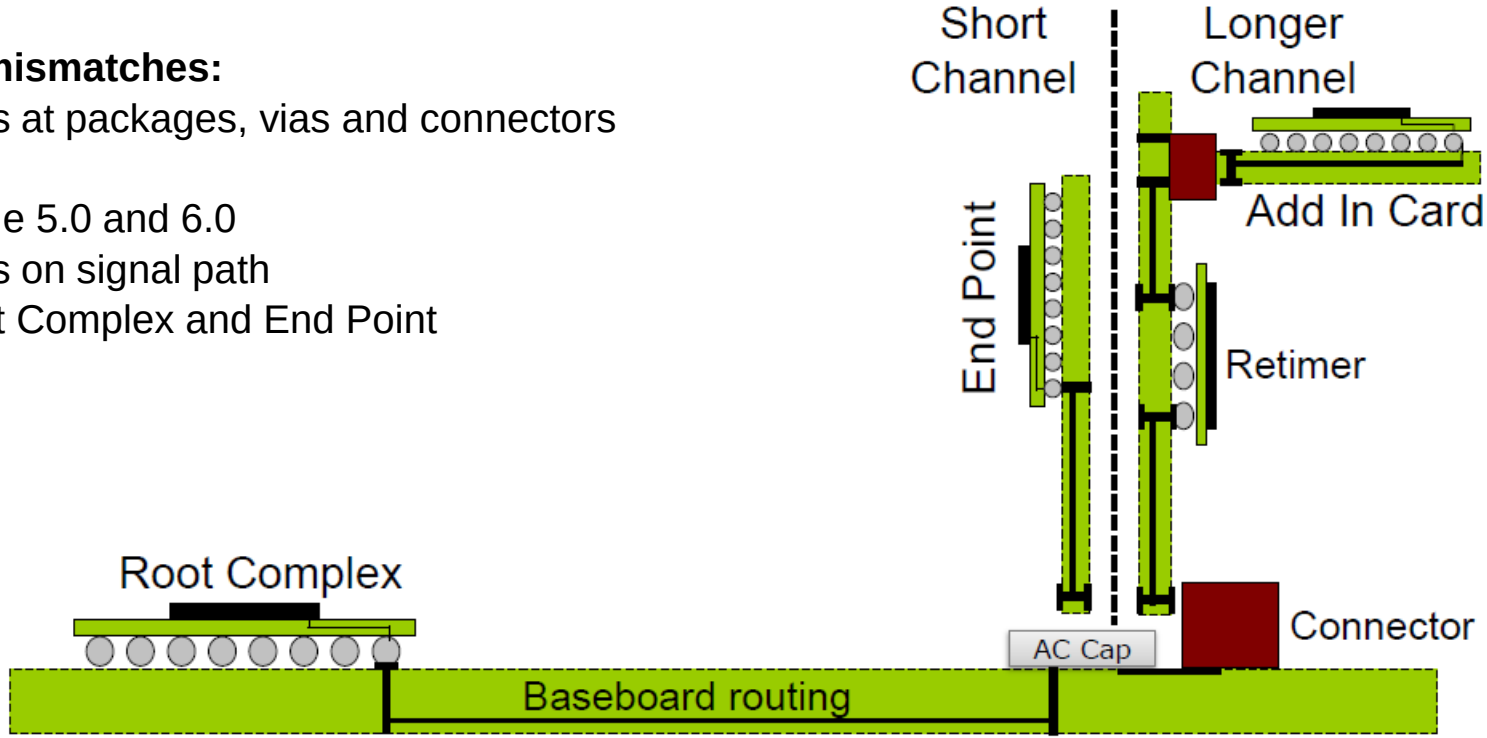


CHALLENGE 2: CHARACTERIZING A TRANSMISSION CHANNEL BETWEEN 2 CHIPS / CHIPLETS

SIGNAL INTEGRITY CHALLENGES IN HIGH-SPEED CHANNELS EXAMPLE: PCIE 5.0 AND 6.0

- **impedance mismatches:**
  discontinuities at packages, vias and connectors

  Example: PCIe 5.0 and 6.0
  discontinuities on signal path
  between Root Complex and End Point



SIGNAL INTEGRITY CHALLENGES IN HIGH-SPEED CHANNELS EXAMPLE: PCIE 5.0 AND 6.0

- **losses and frequency response of PCB material**

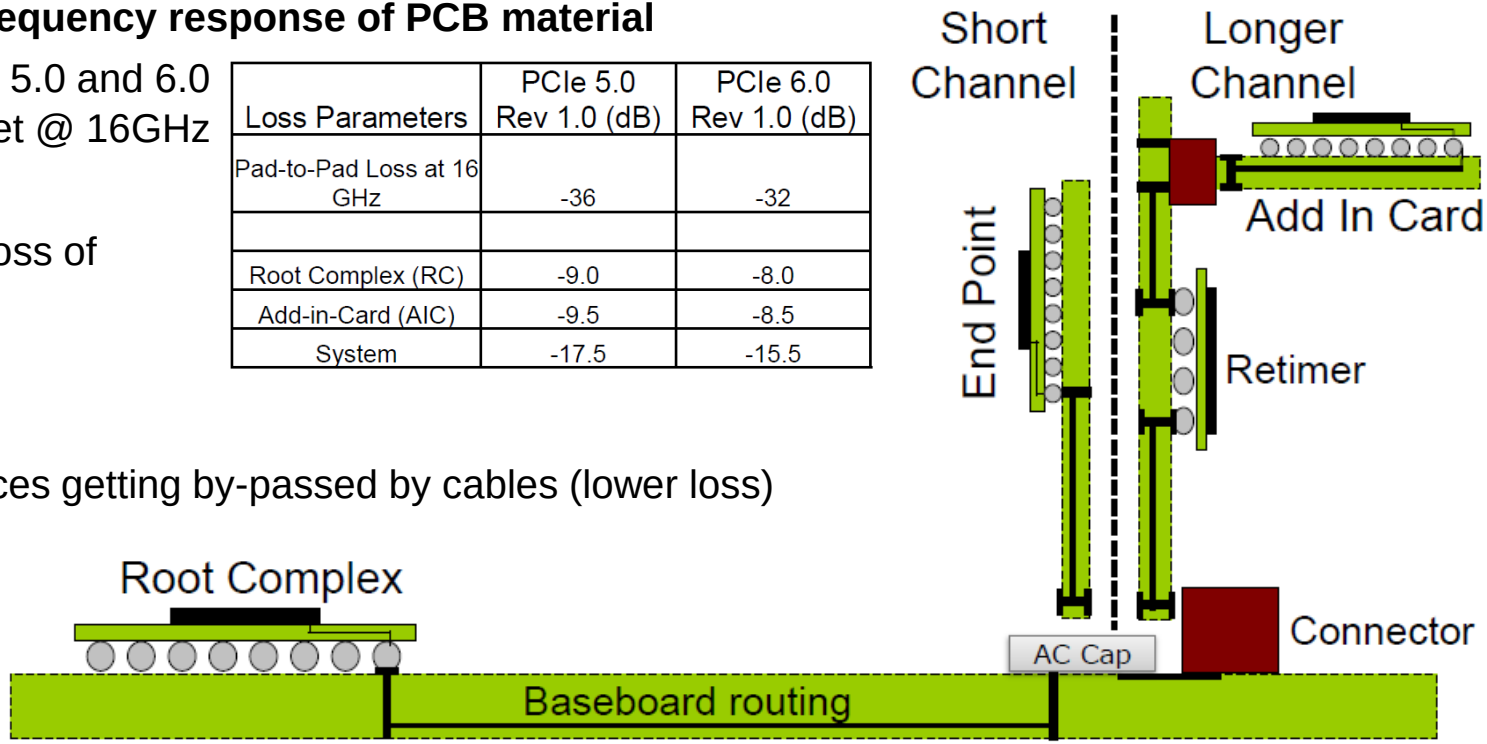
Example: PCIe 5.0 and 6.0 total loss budget @ 16GHz

Loss Parameters	PCIe 5.0 Rev 1.0 (dB)	PCIe 6.0 Rev 1.0 (dB)
Pad-to-Pad Loss at 16 GHz	-36	-32
Root Complex (RC)	-9.0	-8.0
Add-in-Card (AIC)	-9.5	-8.5
System	-17.5	-15.5

requires PCB loss of ≤ 1.0 dB / inch

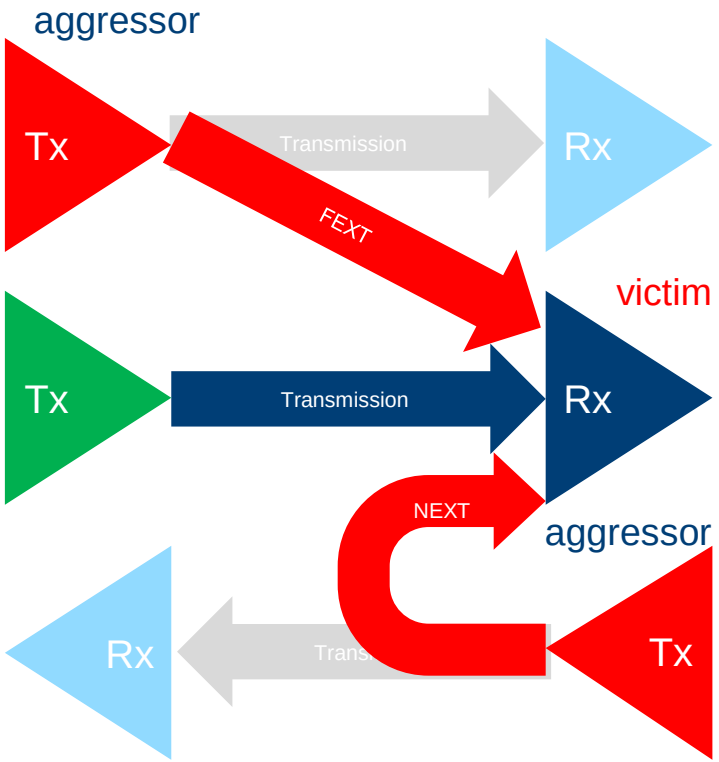
trend:

PCB signal traces getting by-passed by cables (lower loss)



SIGNAL INTEGRITY CHALLENGES IN HIGH-SPEED CHANNELS EXAMPLE: PCIE 5.0 AND 6.0

- crosstalk:
  - near end crosstalk: NEXT
  - far end crosstalk: FEXT
- multiple aggressors: power sum
  - power sum NEXT: PSNEXT or multi-disturber NEXT: MDNEXT
  - power sum FEXT: PSFEXT or multi-disturber FEXT: MDFEXT



TEST PARAMETERS IN PCIE 5.0 / 6.0
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES

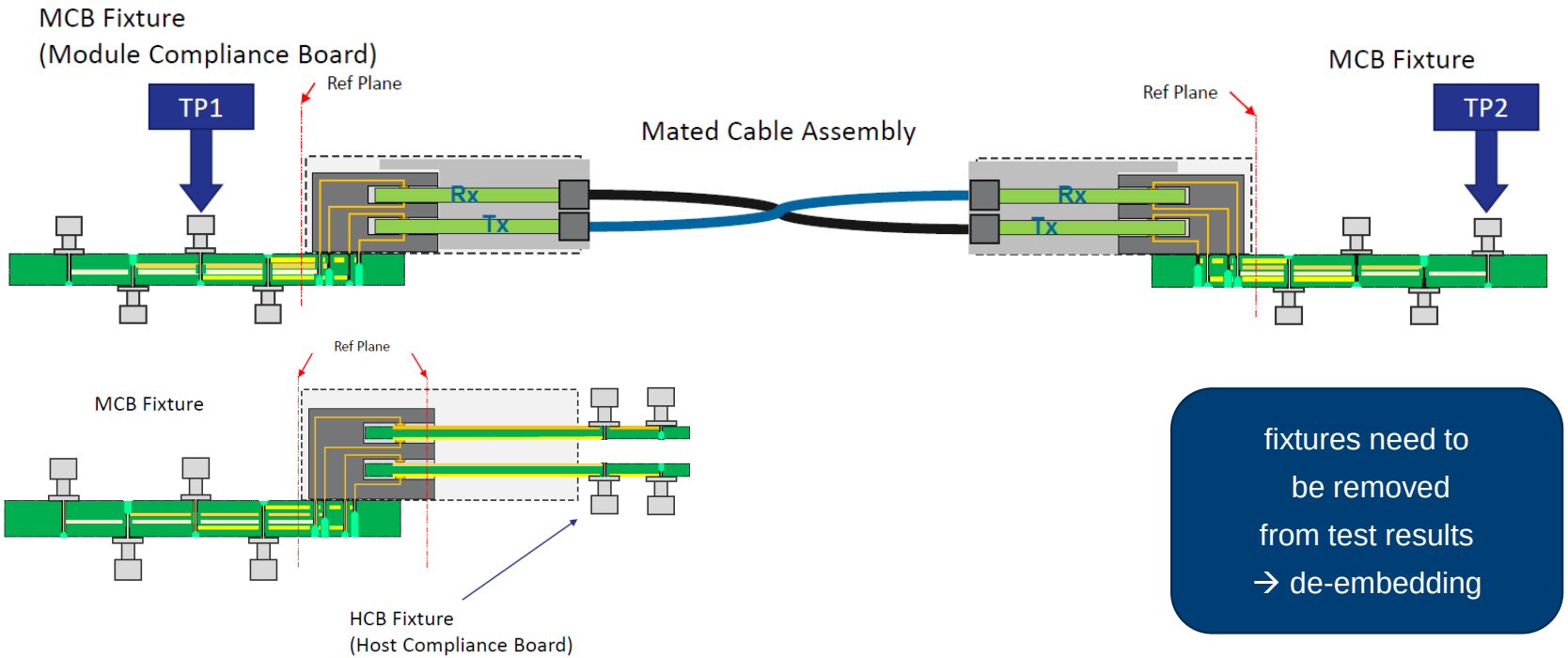
Parameters according to PCIe Specification:

- Differential Insertion Loss (Sdd21): mask check against IL limit mask
- Differential Return Loss (Sdd11 and Sdd22): mask check against RL limit mask
  iRL metric: method of waiver, if RL violates limit mask
- NEXT and PSNEXT (power sum of individual NEXT aggressors): mask check against PSNEXT limit mask
  $ccICN_{NEXT}$ metric: method of waiver, if PSNEXT violates limit mask
- FEXT and PSFEXT (power sum of individual FEXT aggressors): mask check against PSFEXT limit mask
  $ccICN_{FEXT}$ metric: method of waiver, if PSFEXT violates limit mask
- Intra-Pair Skew EIPS (Effective Intra-Pair Skew): limit check
- Inter-Pair Skew (Lane-to-Lane Skew): limit check

Beyond Specification:

- Differential Trace Impedance Profile
- …

REFERENCE PLANE DEFINITION IN PCIe
EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES



fixtures need to
be removed
from test results
→ de-embedding

Source: PCI-SIG Electrical Work Group (EWG): PCIe 5.0/6.0 External Cable Specification (in progress)

TEST PARAMETERS IN IEEE 802.3ck
EXAMPLE: 802.3ck COPPER CABLE ASSEMBLIES (CR)

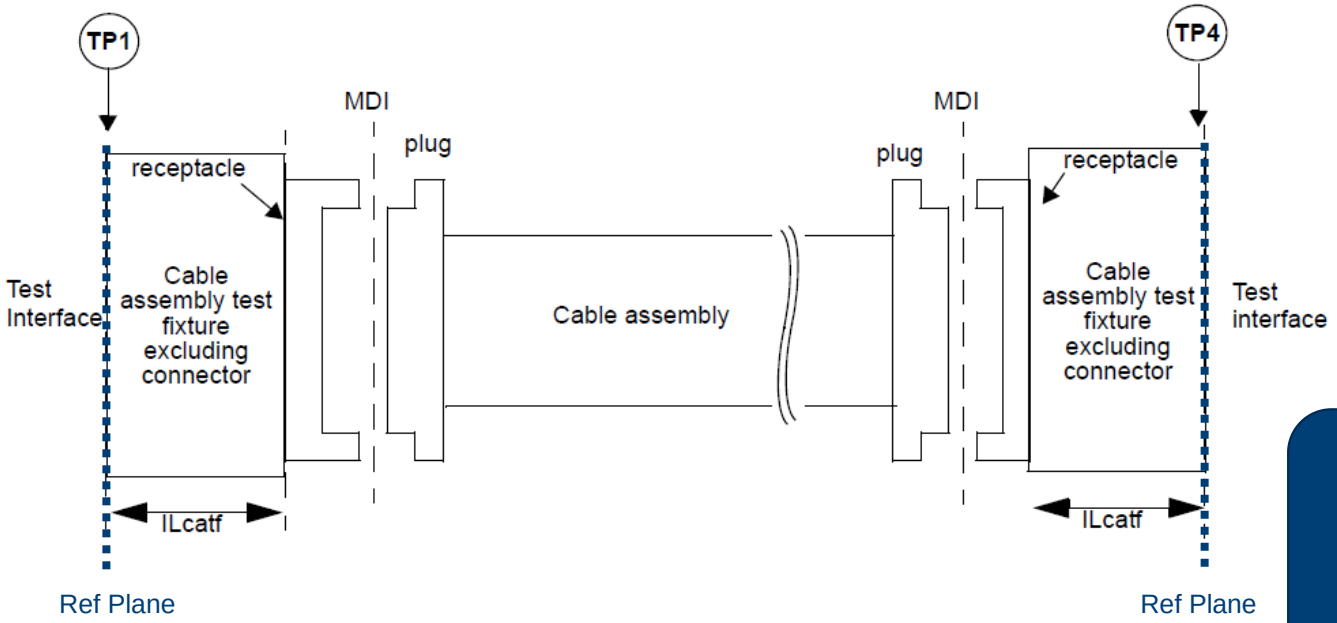
Parameters according to IEEE Specification:

- Differential Insertion Loss (Sdd21): mask check against ILdd limit mask
- Differential-Mode to Common-Mode Return Loss (Scd11 and Scd22): mask check against RLcd limit mask
- Differential-Mode to Common-Mode Insertion Loss (Scd21) minus Differential Insertion Loss (Sdd21): mask check against ILcd-ILdd limit mask
- Common-Mode to Common-Mode Return Loss (Scc11 and Scc22): mask check against RLcc limit mask
- Metrices:
  - Channel Operating Margin (COM)
  - for cable assemblies with COM < 4dB:
    Effective Return Loss (ERL)

Beyond Specification:

- Differential Trace Impedance Profile
- …

REFERENCE PLANE DEFINITION IN IEEE 802.3
EXAMPLE: 802.3ck COPPER CABLE ASSEMBLIES (CR)

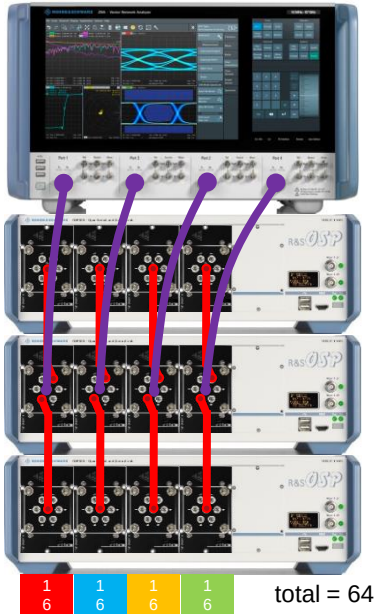


fixture are included
in test results
→ no de-embedding

Source: IEEE Std 802.3bj-2014

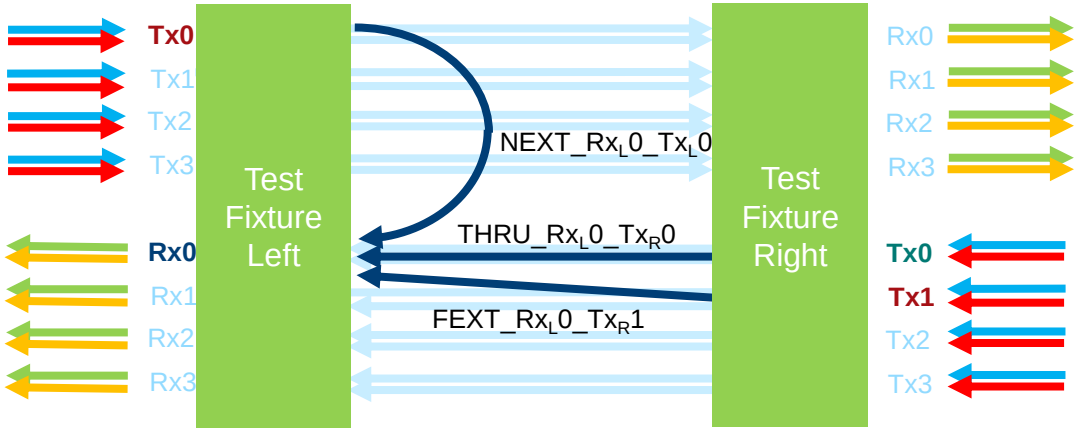
VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: GENERAL CONSIDERATIONS

Measurements:
automation with switch matrix:
example for PCIe x8



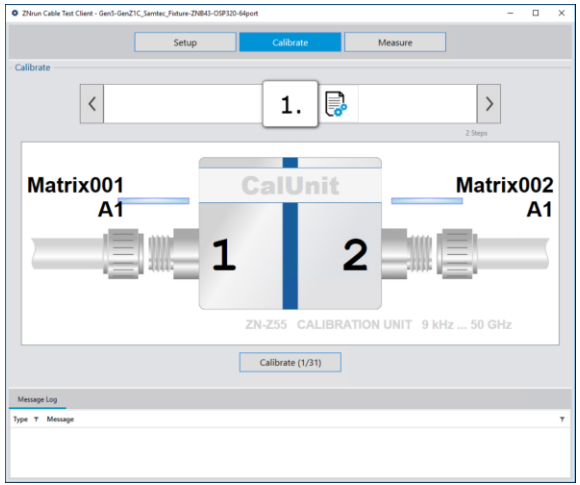
total = 64 ports

	PCIe x4	PCIe x8	PCIe x16
number of lanes (Tx + Rx)	8	16	32
number of ports for full testing (all lanes and all crosstalk combinations)	32	64	128
number of 4-port measurements for full testing (all lanes and all crosstalk combinations)	8 x THRU 4 x 4 = 16 x NEXT_L 4 x 4 = 16 x NEXT_R 3 x 4 = 12 x FEXT_L 3 x 4 = 12 x FEXT_R total: 64 4-port meas.	16 x THRU 8 x 8 = 64 x NEXT_L 8 x 8 = 64 x NEXT_R 7 x 8 = 56 x FEXT_L 7 x 8 = 56 x FEXT_R total: 256 4-port meas.	32 x THRU 16 x 16 = 256 x NEXT_L 16 x 16 = 256 x NEXT_R 15 x 16 = 240 x FEXT_L 15 x 16 = 240 x FEXT_R total: 1024 4-port meas.

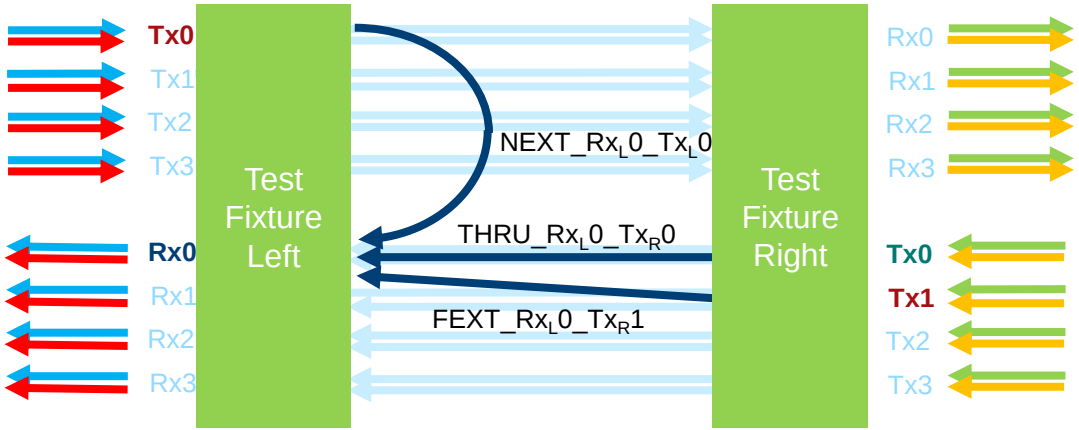


VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: GENERAL CONSIDERATIONS

Calibration:
automation of calibration
example for PCIe x4 w. R&S ZNrun

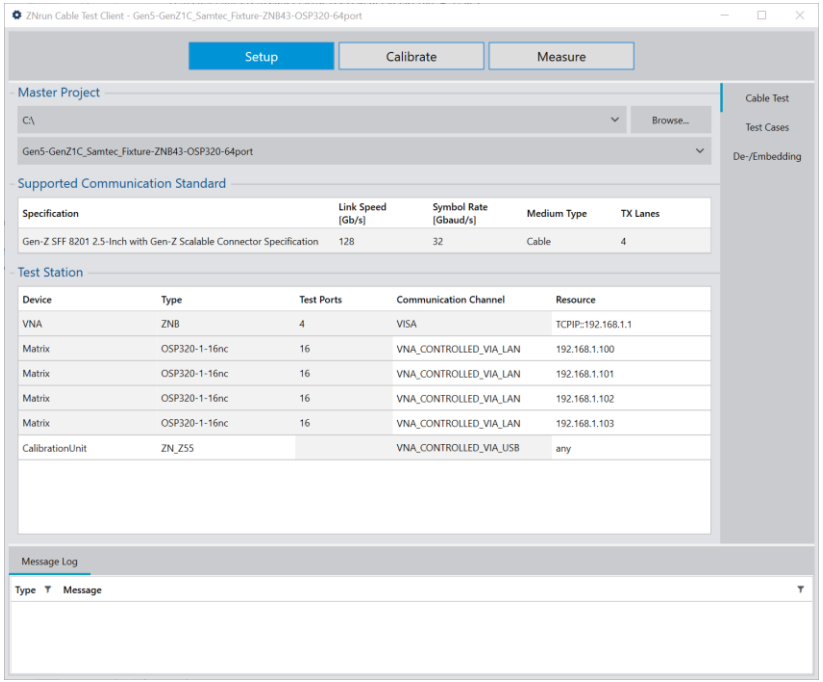


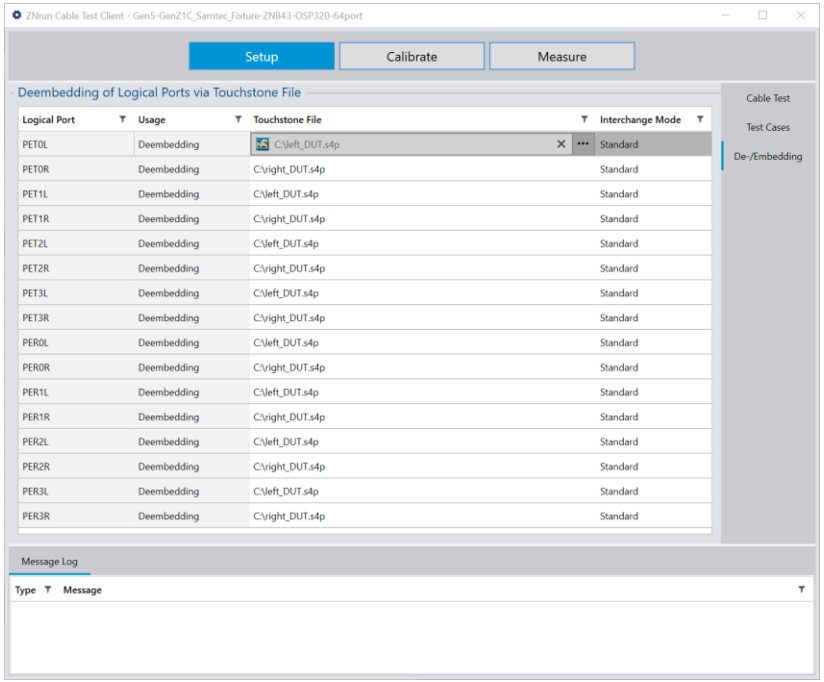
	PCIe x4	PCIe x8	PCIe x16
number of lanes (Tx + Rx)	8	16	32
number of ports for full testing (all lanes and all crosstalk combinations)	32	64	128
number of 4-port measurements for full testing (all lanes and all crosstalk combinations)	64 4-port groups:	256 4-port groups:	1024 4-port groups:
standard calibration (3 connections per 4-port)	64 x 3 = 192	256 x 3 = 768	1024 x 3 = 3072
optimized calibration	**31**	**63**	**127**



VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: TEST AUTOMATION W. ZNRUN-K440

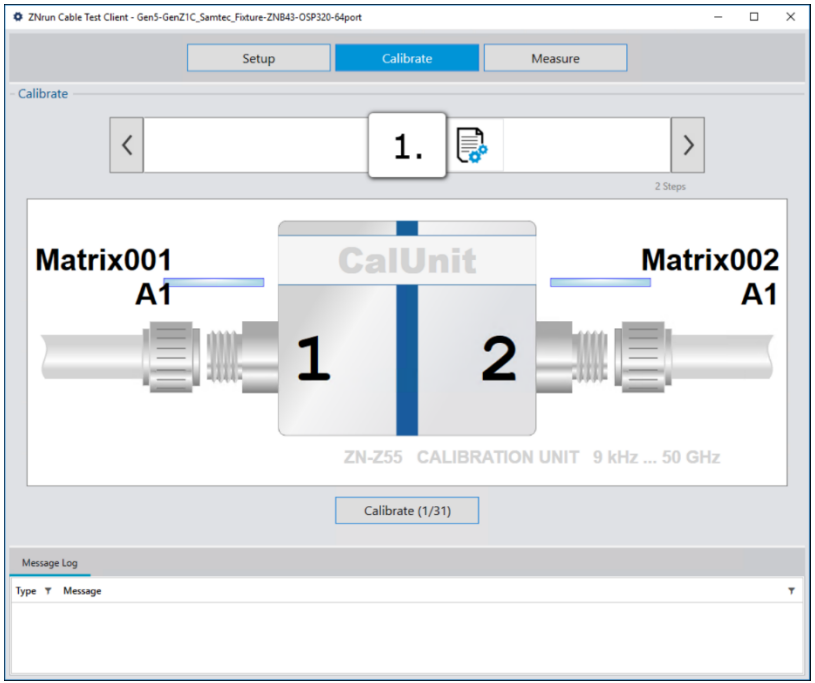
1. Setup





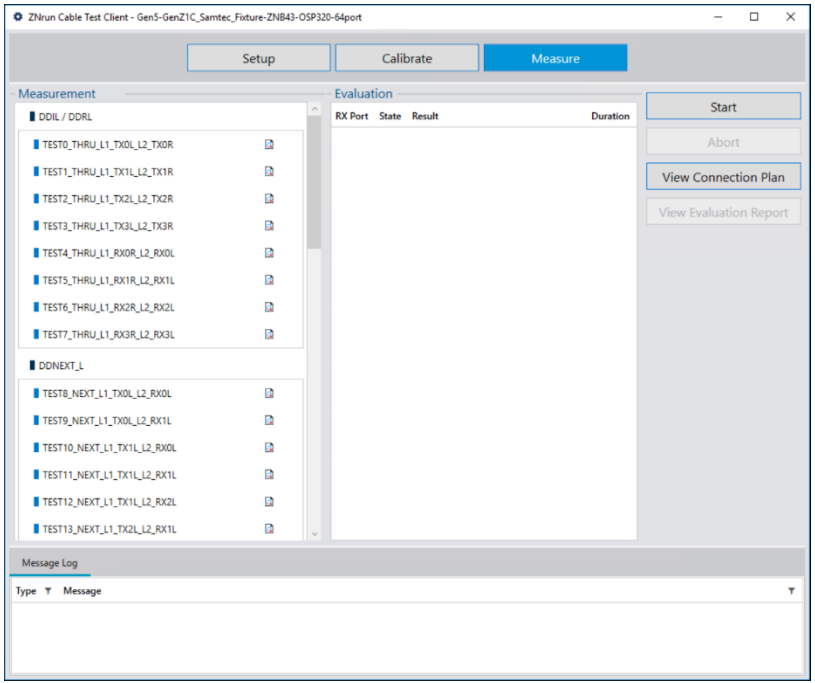
VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: TEST AUTOMATION W. ZNRUN-K440

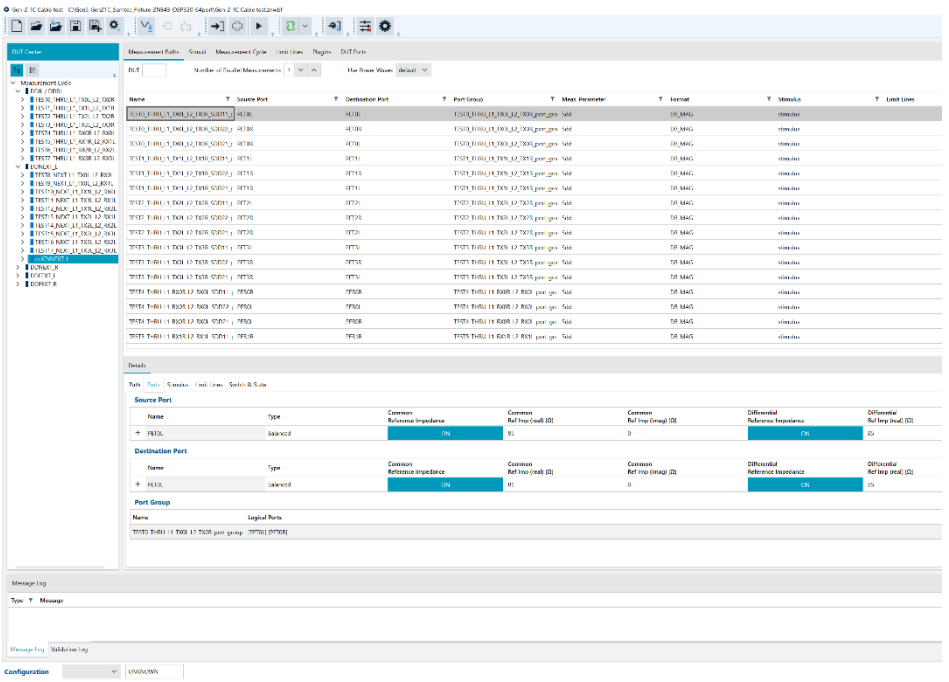
2. Calibration



VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: TEST AUTOMATION W. ZNRUN-K440

3. Measurement incl. Workbench Editor





VERIFICATION OF PCIE 5.0 / 6.0 CABLES AND CONNECTORS: TEST AUTOMATION W. ZNRUN-K440

4. Test Report

ROHDE&SCHWARZ
Make ideas real

ZNrun Cable Test

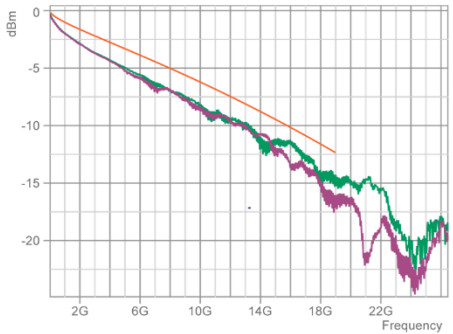
Measurement Results (S-Parameters)	Evaluation Results (iRL, ccICNNEXT, ccICNFEXT)	Overall Result
PASS	PASS	PASS

Supported Communication Standard

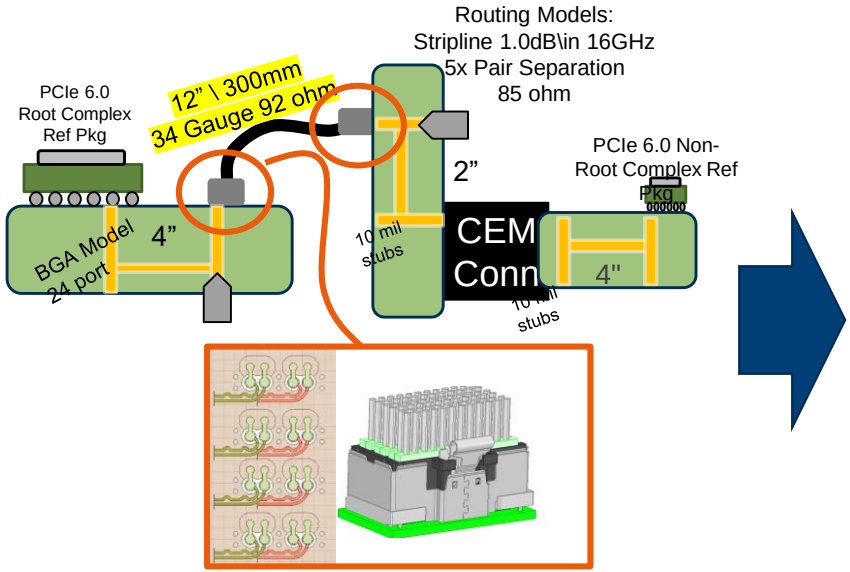
Specification	Link Speed [Gb/s]	Symbol Rate [GT/s]	Medium Type	TX Lanes
Gen-Z SFF 8201 2.5-Inch with Gen-Z Scalable Connector Specification	128	32	Cable	4

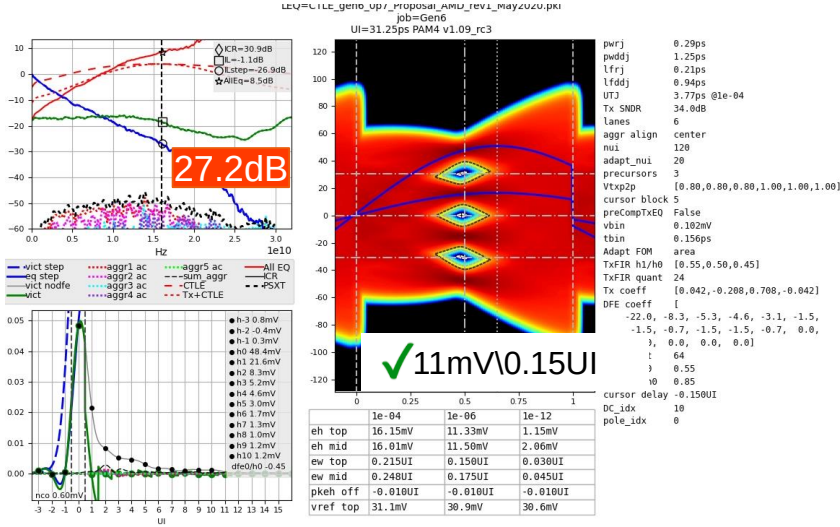
ROHDE&SCHWARZ
Make ideas real

Chart 1: Differential-Mode Insertion Loss

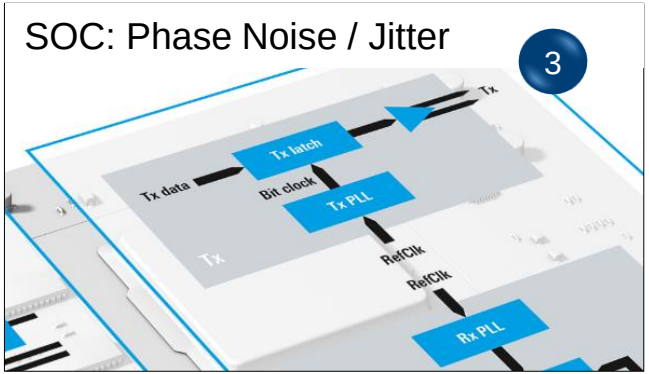


FURTHER METHODS:
EXAMPLE FOR PCIE 6.0 - CHANNEL SIMULATION W. SEASIM

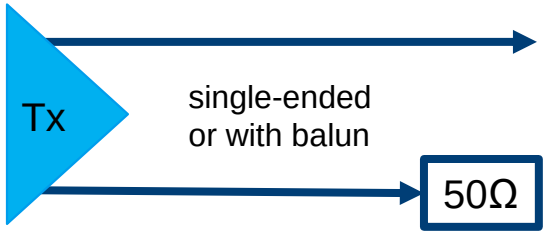




Source: PCI-SIG DevCon 2023

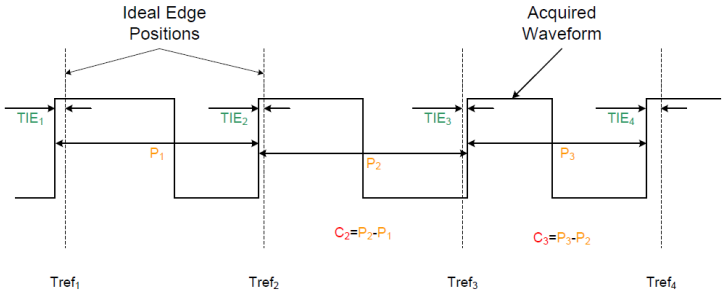


quasi-ideal
RefClk



CHALLENGE 3: MEASURING TRUE PHASE NOISE AND JITTER IN HIGH-SPEED DIGITAL DESIGNS

RJ MEASUREMENT IN TIME DOMAIN: OSCILLOSCOPE



- TIE Jitter Measurement:
  - Track
  - Histogram
  - Spectrum

$$j_{TIE}(n) = (t_n - t_{REF_n})$$

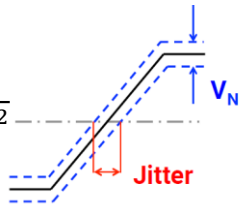
- Sampled Measurement (e.g. rising edge)
  → sampling with clock frequency
  → TIE jitter spectrum shows aliasing products (Nyquist frequency)

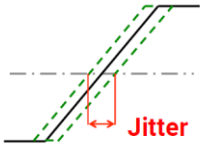
- Reference: t_{REF_n}
  → calculation based on ideal signal or selected CDR
  → TIE result includes effect of CDR Transfer Function (HP Filter)

- Pattern Types: all, but RJ best extracted with clock-like 1010 signal

- **Limitation by Scope Jitter Measurement Floor**
  High Sensitivity on Signal Slew Rate

$$\sqrt{(Noise\ /\ SlewRate)^2 + (Intrinsic\ Jitter)^2}$$





RJ MEASUREMENT IN FREQUENCY DOMAIN: PHASE NOISE ANALYZER

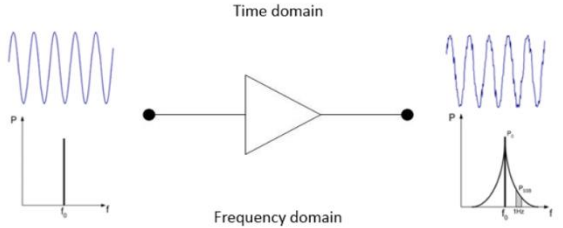
- Phase Noise Measurement:
  - Phase Noise
  - Phase Jitter
    → integrate phase noise in offset-range
    → divide by clock-frequency ω_0
- Continuous Measurement
  → phase noise spectrum shows no aliasing products
  → for comparability with TIE jitter measurement: measurement to high offsets + folding into Nyquist
- Reference: Ideal Signal
  → result does not include effect of CDR Transfer Function (HP Filter)
  → for comparability with TIE jitter measurement: apply CDR weighting
- Pattern Types: requiring alternating 1010 signal, results for RJ and PJ
- **Made for Phase Noise Testing:**
  → Outstanding Phase Noise / Jitter Performance

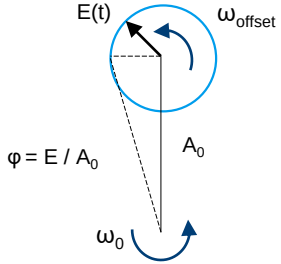
Ideal Signal
$V(t) = A_0 \sin \omega_0 t$

Where:
A_0 = nominal amplitude
ω_0 = nominal frequency

Real-world Signal
$V(t) = (A_0 + E(t)) \sin(\omega_0 t + \varphi(t))$

Where:
E(t) = random amplitude changes
Φ(t) = random phase changes

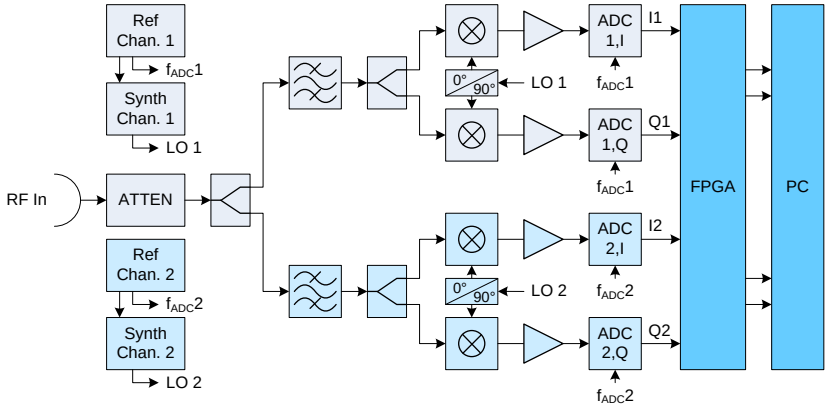




RJ MEASUREMENT IN FREQUENCY DOMAIN: PHASE NOISE ANALYZER

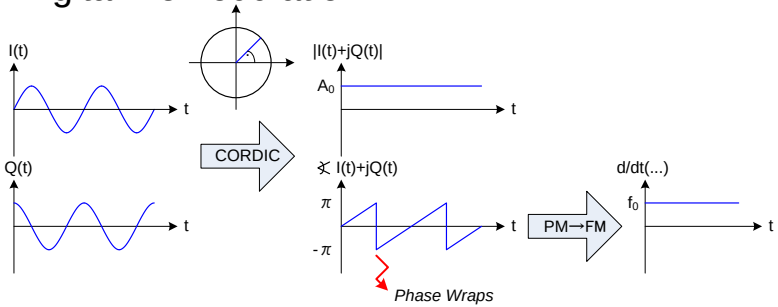
FSWP Architecture

► Signal Path

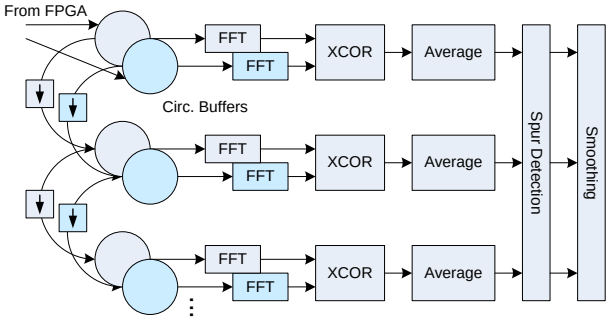


FSWP Signal Processing

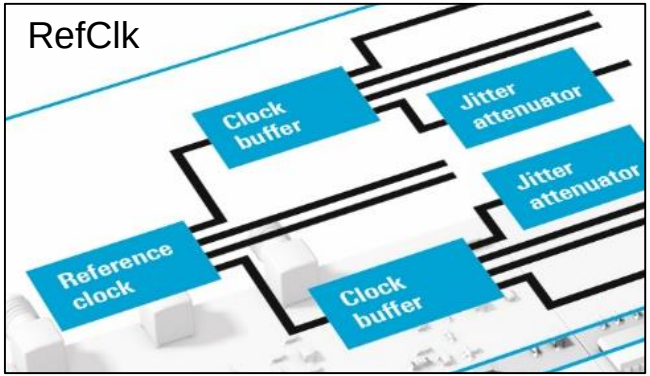
► Digital Demodulation



► Cross-Correlation



PHASE NOISE AND JITTER MEASUREMENT: SETUP FOR ULTRA-LOW JITTER REFCLKs



RefClk

100 MHz for PCIe

50Ω

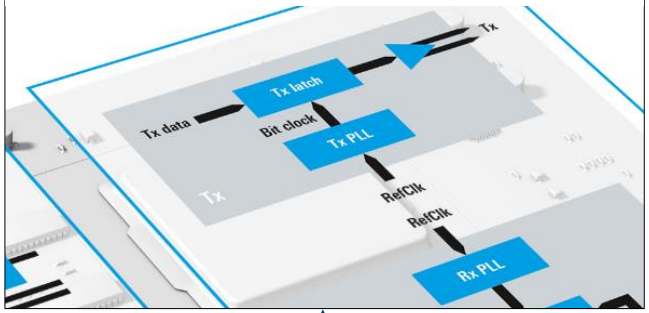
single-ended
or w. balun

R&S FSWP
- phase noise and RJ measurement
- with and without SSC
- weighting with behavioral CDR

PHASE NOISE AND JITTER MEASUREMENT: SETUPS FOR ULTRA-LOW JITTER SOCS

Setup 1: below 50 GHz

SOC: Phase Noise / Jitter



RefClk

R&S SMA100B:
quasi-ideal PCIe RefClk
to measure true SOC performance

16 GHz for PCIe 5.0 / 6.0
32 GHz for PCIe 7.0
53 GHz for IEEE 802.3dj
56 GHz for OIF CEI-224

Tx

single-ended
or with balun

50Ω

R&S FSWP
- phase noise and RJ measurement
- with and without SSC
- weighting with behavioral CDR

PHASE NOISE AND JITTER MEASUREMENT: EXPERIMENT FOR PCIE 7.0

Signal level @ FSWP: -16 dBm
- 400 mVpp at die → -4 dBm
- 12 dB attenuation from die via package to test equipment → -16 dBm

R&S SMA100B:
quasi-ideal PCIe 7.0 signal source
- 32 GHz
- ultra-low phase noise
- ultra-low wideband noise

R&S FSWP
- phase noise and RJ measurement

PHASE NOISE AND JITTER MEASUREMENT: EXPERIMENT FOR PCIE 7.0

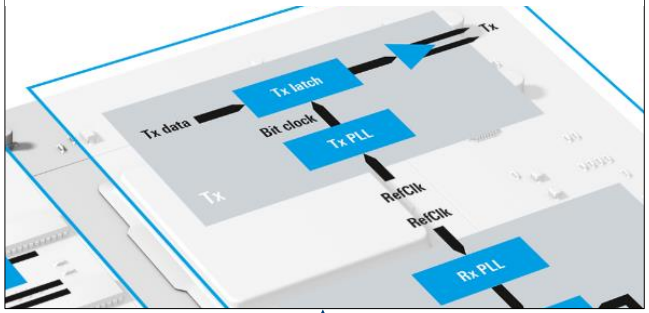
Measurement:

– phase noise measurement to 18 GHz offset

PHASE NOISE AND JITTER MEASUREMENT: SETUPS FOR ULTRA-LOW JITTER SOCS

Setup 2: above 50 GHz

SOC: Phase Noise / Jitter



RefClk

R&S SMA100B:
quasi-ideal PCIe RefClk
to measure true SOC performance

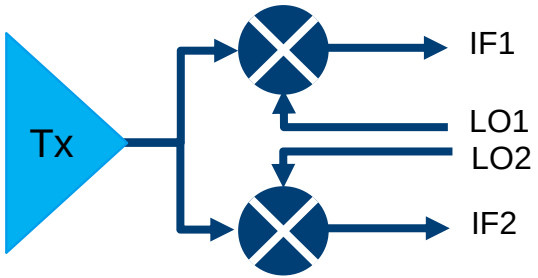
16 GHz for PCIe 5.0 / 6.0
32 GHz for PCIe 7.0
53 GHz for IEEE 802.3dj
56 GHz for OIF CEI-224

Tx

single-ended
or with balun

50Ω

R&S FSWP with 2 x FS-Z75
- phase noise and RJ measurement
- weighting with behavioral CDR



PHASE NOISE AND JITTER MEASUREMENT: ULTRA-LOW JITTER PLLS

Models	Frequency range	1dB compression	Conversion loss	RF port	LO harmonic number
FS-Z60 Order number 1048.0171.02	40 GHz – 60 GHz	0 dBm	15 dB	WR19	4
FS-Z75 Order number 3638.2240.02	50 GHz – 75 GHz	-5 dBm	20 dB	WR15	6
FS-Z90 Order number 3638.2270.02	60 GHz – 90 GHz	-6 dBm	16 dB	WR12	6
FS-Z110 Order number 3638.2292.02	75 GHz – 110 GHz	-6 dBm	23 dB	WR10	8
FS-Z140 Order number 3622.0708.02	90 GHz – 140 GHz	-3 dBm	28 dB	WR08	10
FS-Z170 Order number 3622.0714.02	110 GHz – 170 GHz	-3 dBm	30 dB	WR06	12
FS-Z220 Order number 3593.3250.02	140 GHz – 220 GHz	-5 dBm	32 dB	WR5.1	16
FS-Z325 Order number 3593.3267.02	220 GHz – 325 GHz	-5 dBm	40 dB	WR3.4	18

PHASE NOISE AND JITTER MEASUREMENT: EXPERIMENT FOR 224 GBPS SERDES

Signal level @ WG splitter input: -20 dBm
- 400 mVpp at die → -4 dBm
- 16 dB attenuation from die via package to WG splitter input → -20 dBm

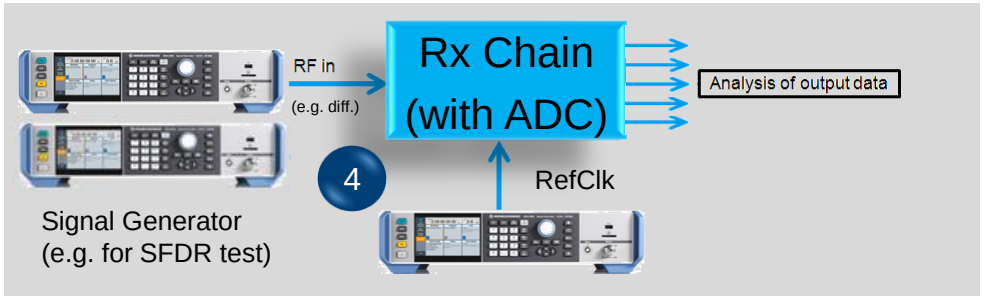
R&S SMA100B:
quasi-ideal OIF CEI-224G signal source
- 56 GHz
- ultra-low phase noise
- ultra-low wideband noise

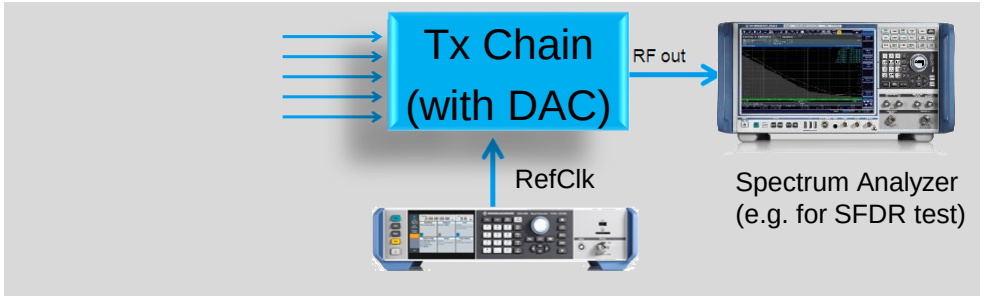
R&S FSWP
- phase noise and RJ measurement

PHASE NOISE AND JITTER MEASUREMENT: EXPERIMENT FOR 224 GBPS SERDES

Measurement:

- phase noise measurement to 10 GHz offset

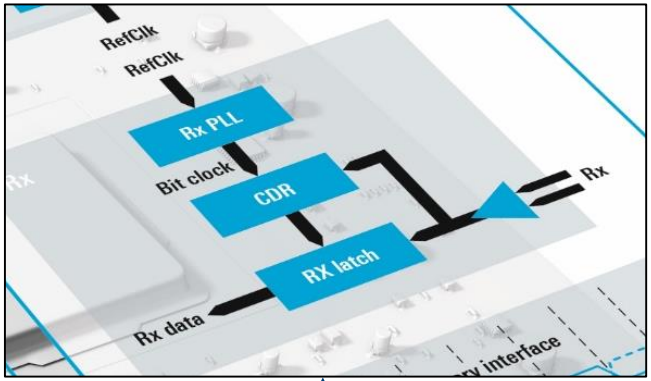




CHALLENGE 4: MEASURING TRUE ADC AND DAC PERFORMANCE AND FRONTEND DISTORTIONS

ADC VERIFICATION WITH SMA100B: TESTING SPURIOUS FREE DYNAMIC RANGE (SFDR)

Setup 1a: below 67 GHz – 1 x SG + balun, 1-tone



RefClk

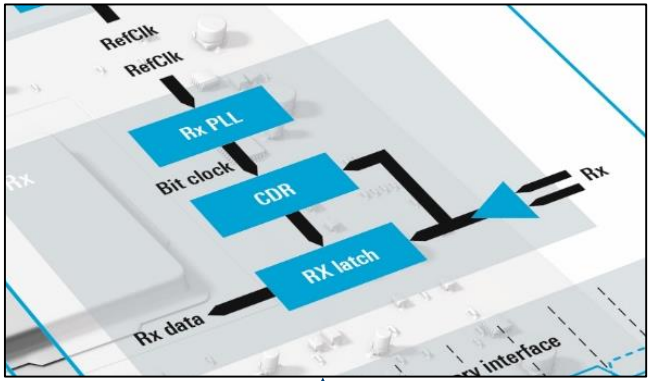
Rx

Balun

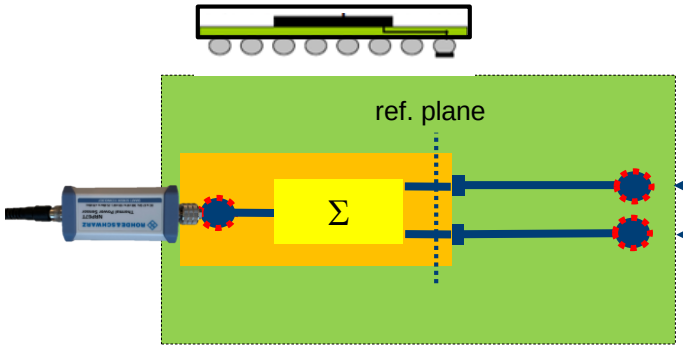
R&S SMA100B:
quasi-ideal ADC stimulus
quasi-ideal RefClk

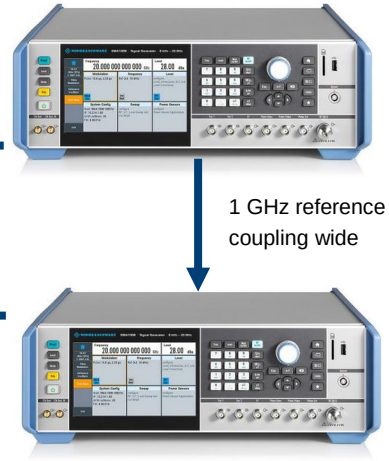
ADC VERIFICATION WITH SMA100B: TESTING SPURIOUS FREE DYNAMIC RANGE (SFDR)

Setup 1b: below 67 GHz; 2 x SG → 180° phase alignment at ref. plane, 1-tone



RefClk



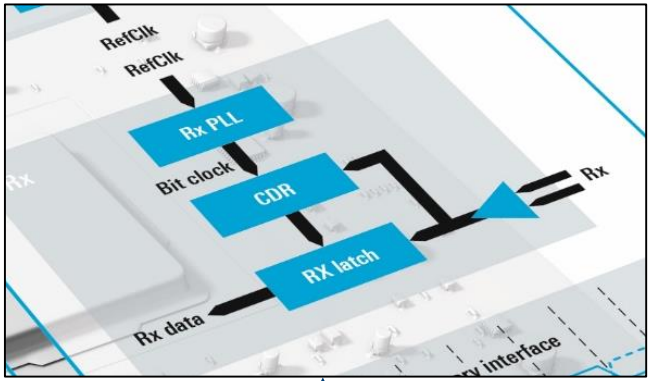


1 GHz reference coupling wide

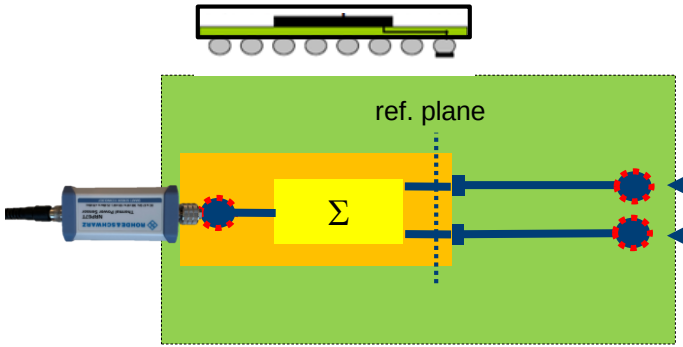
2 x R&S SMA100B:
quasi-ideal ADC stimulus
quasi-ideal RefClk

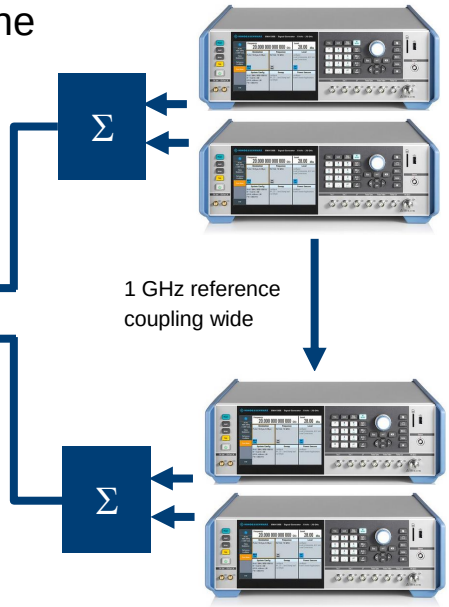
ADC VERIFICATION WITH SMA100B: TESTING SPURIOUS FREE DYNAMIC RANGE (SFDR)

Setup 1c: below 67 GHz; 2 x SG → 180° phase alignment at ref. plane, 2-tone



RefClk

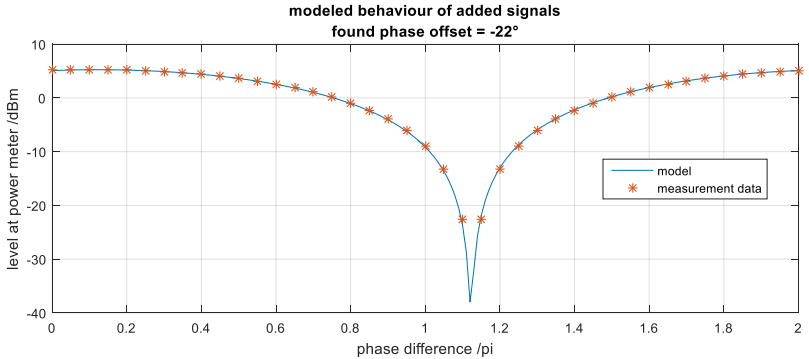




2 x R&S SMA100B:
quasi-ideal ADC stimulus
quasi-ideal RefClk

PHASE ALIGNMENT OF DIFFERENTIAL SIGNAL DESCRIPTION OF METHOD

1. Both instruments are set to desired frequency and level
2. Script performs level measurement to determine SG power levels P1 and P2.
3. Model is fitted to measured power levels to gain phase offset



4. 180° phase offset can be achieved at reference plane

CHALLENGE 5: ANALYZING AND DEBUGGING POWER REFERENCE DESIGNS AND POWER INTEGRITY PROBLEMS

POWER MANAGEMENT / POWER INTEGRITY TEST
DEDICATED TOOLS FOR VALIDATION & DEBUG TEST

The Right Scope

- 4 / 8 channels and more
- Fast update rate: 4.5 Mwfms / s
- High resolution: 12 bit ADC (18 bit in HD mode)
- > 45 k FFT / s
- High internal DC offset for high resolution on power rail ripple (2V @ 0.5 mV/div)
- Built-in AWG (option)

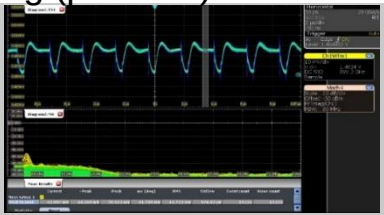
Specialized Probes

- Power Rail Probe
  - Bandwidths: 2 GHz / 4 GHz
  - Low noise with 1:1 attenuation
  - Extended offset range
  - DC meter to find offset value
- Current probes
- …

Analysis Functions

Typical measurements

- Load step response, ripple and drift measurements
- Power-up/down sequencing
- PSRR / PSNR testing
- EMI / crosstalk debugging (frequency domain)
- Control bus analysis and timing (protocol)



POWER MANAGEMENT FOR SOCS AND RFSOCS: INDUSTRY TRENDS AND CHALLENGES

- Growing demand of high-performance SoCs and RFSoCs for use in
  - data centers
  - fixed and wireless network infrastructure
  - modern ADT applications
- Power delivery solutions need to provide a high number of low-voltage / high-current power rails with
  - precisely controlled sequencing for power-up and power-down
  - low voltage ripple and fast response on load steps
  - high efficiency
- Power delivery designs use a combination of linear and switching regulator technologies
  - power rails with high currents: increasing use of multi-phase buck converters (instead of single-phase buck converters)
    → test of phase alignment / phase management requires oscilloscopes with >> 4 channels
  - power rails with low currents and requirements for low noise and ripple: use of low-dropout linear regulators (LDOs)
    → test of Power Supply Rejection Ratio (PSRR)
  - test of power sequencing and power rail disturbances
    → requires oscilloscopes with > 4 channels, high resolution and power rail probes with DC offset and built-in DC meter

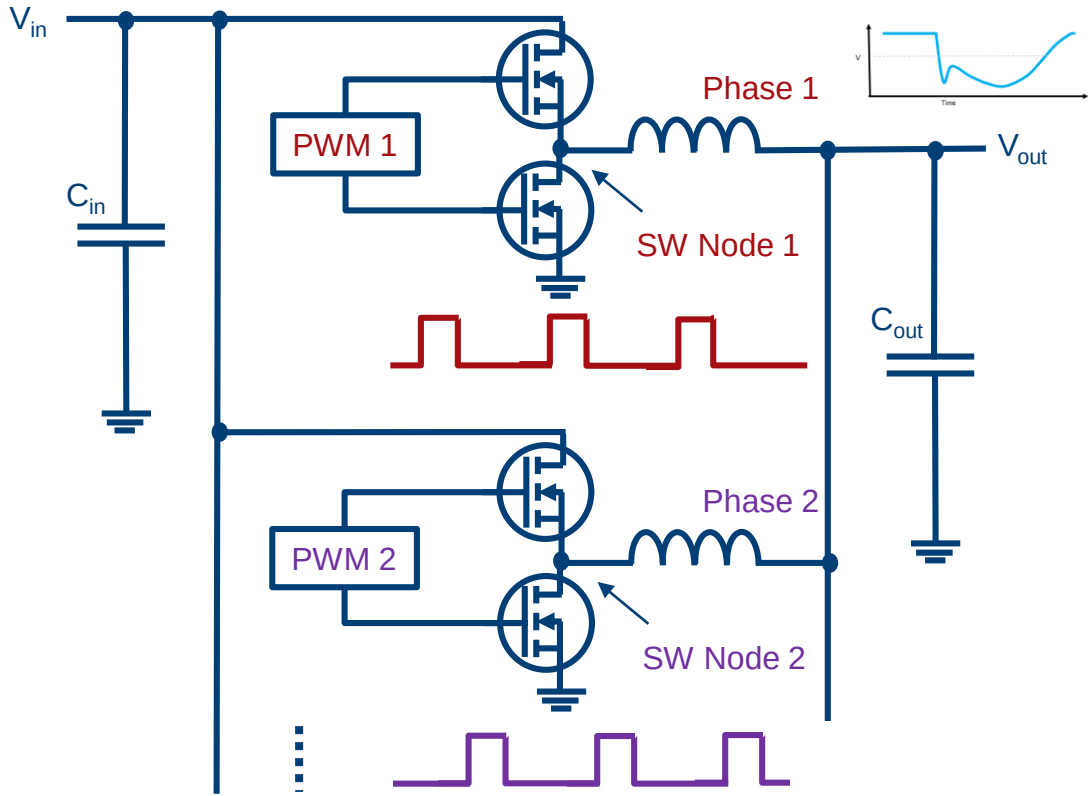
MULTI-CHANNEL MEASUREMENTS ON POWER DESIGNS WITH MULTI-PHASE BUCK CONVERTERS

Multi-Channel Analysis:

- input voltage: V_{in}
- output voltage: V_{out}
- various switch node voltages
- various inductor currents
- control bus analysis, incl. decoding
- power sequencing of SOC power rails

Multi-Domain Analysis

- Time Domain
- Frequency Domain
- Protocol Domain



POWER SUPPLY REJECTION RATIO (PSRR) MEASUREMETS ON LOW-DROPOUT LINEAR REGULATORS (LDOS)

Power Supply

HMP4040

Internal Function Generator (MXO5-B6)

(1 mHz to 100 MHz)

Injector

Power Rail (In)

MXO5

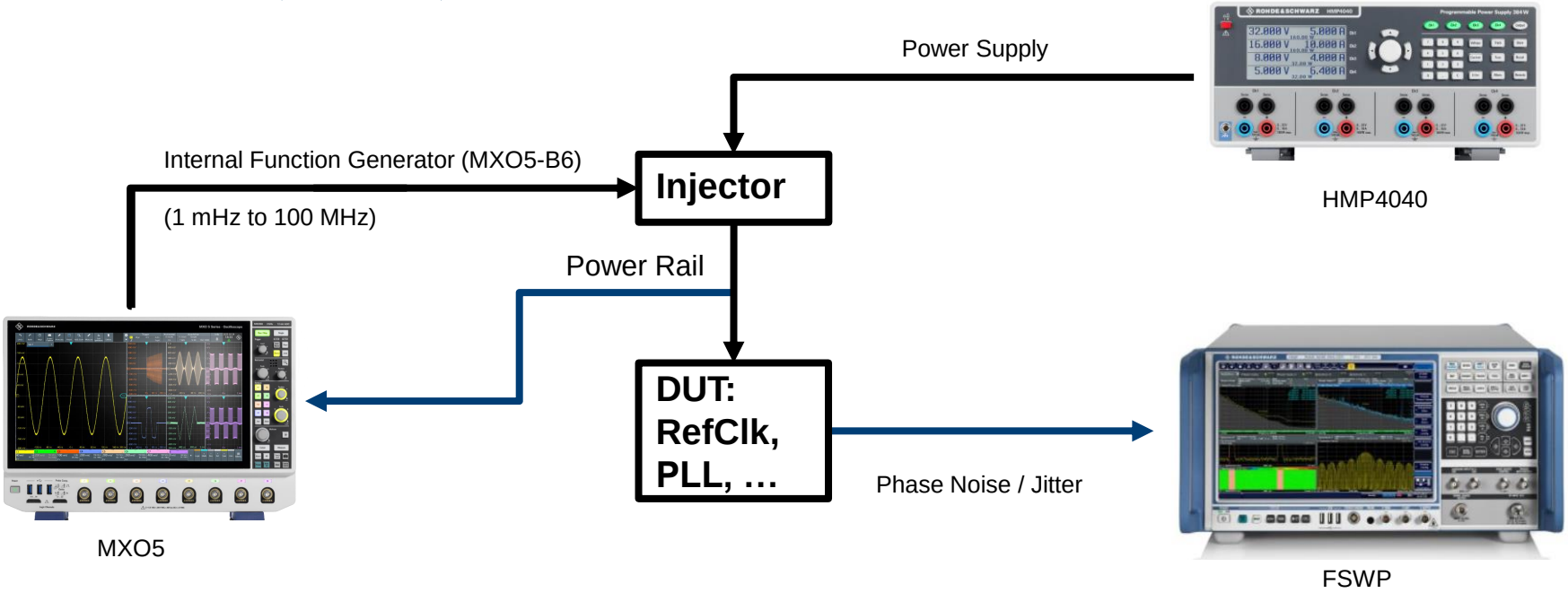
DUT: LDO

Power Rail (Out)

$$PSRR = 20 \log \frac{Ripple_{In}}{Ripple_{Out}}$$

injection of ripple / noise on DUT power rails

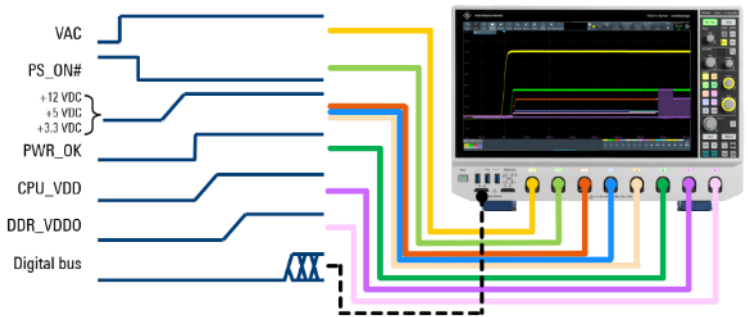
POWER SUPPLY NOISE REJECTION (PSNR) MEASUREMENT ON REFCLKs, PLLs, etc.



injection of ripple / noise on DUT power rails

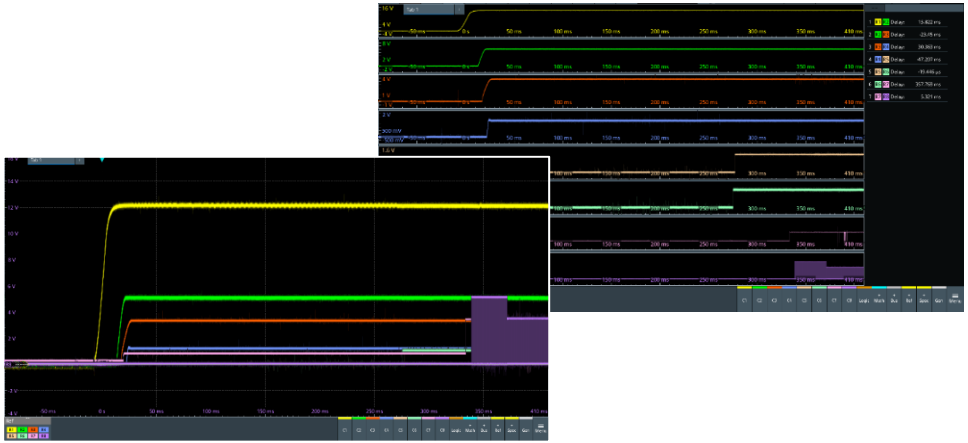
testing of related degradations of phase noise / jitter performance

VERIFICATION OF POWER SEQUENCING IN POWER DELIVERY DESIGNS WITH MULTIPLE POWER RAILS

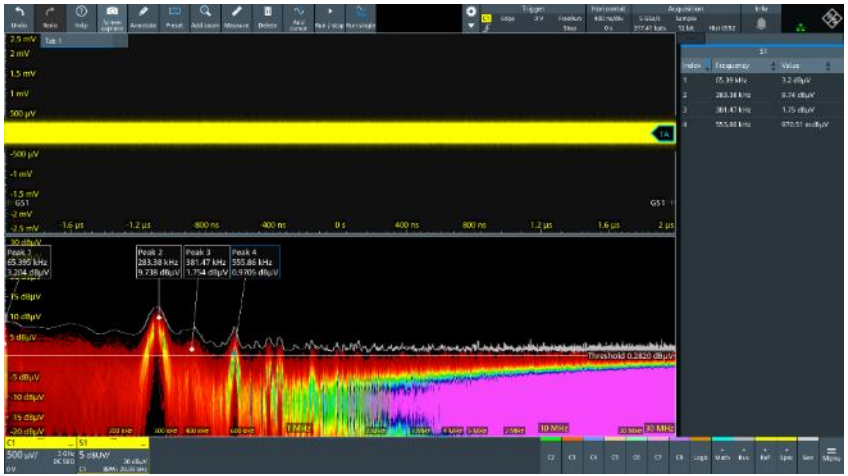


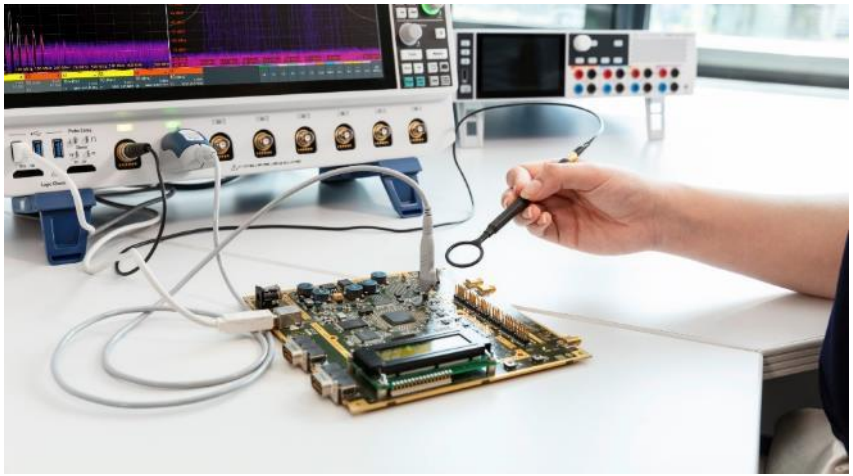
Sampling rate	Capture Duration (500 Mpoints)	Capture Duration (1Gpoints)
5 Gsample/s	100 ms	200 ms
500 Msample/s	1 s	2 s
5 Msample/s	100 s	200 s
8 Ksample/s	17h 21m 40s	1d 10h 43m 20s

- Multiple channels to see more events
- Deep record length for longer observations
- Flexible and intuitive waveform setup
- Configurable delay measurement setup



CROSSTALK ANALYSIS AND EMI DEBUGGING WITH FAST FFT FUNCTIONALITY





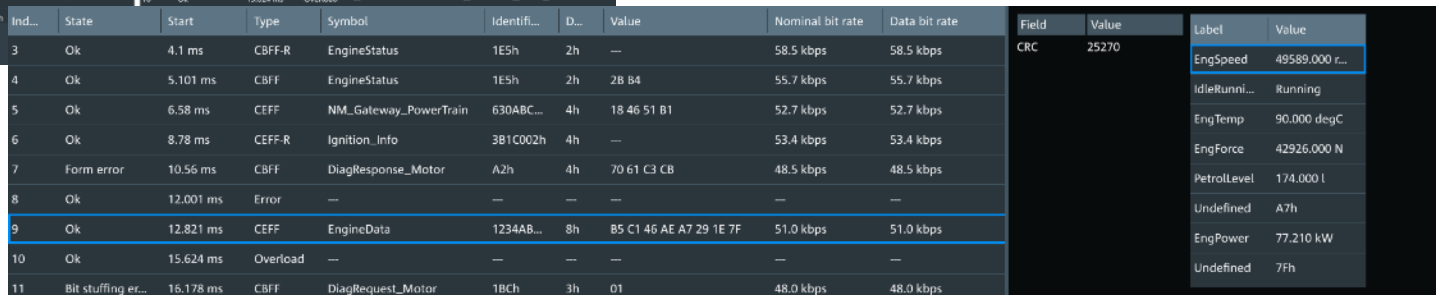
- Standard fast spectrum with 45k FFTs/second
- Support log-log scale and dBuV display of unit
- Peaklist, min/max-hold and intensity grading

HZ-17 Near Field Probes support 30MHz to 3GHz
HZ-16 Amplified extend HZ-17 down to 9kHz

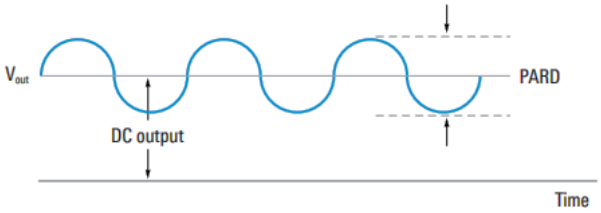
RESPONSE TIME MEASUREMENT ON CONTROL MESSAGES: TRIGGER & DECODE ON LOW-SPEED SERIAL BUSES

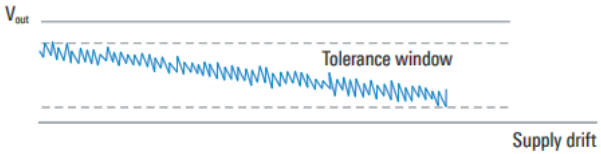
- Dual Path Protocol for correct decode even when low in sample rate
- Support symbolic decode with additional detail for complex protocols

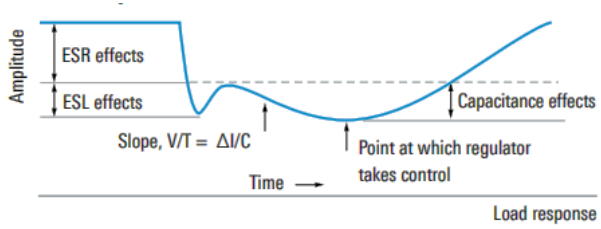
Options		
MXO5-K510	Low speed serial buses	I²C, SPI, RS-232, UART
MXO5-K520	Automotive buses	LIN, CAN-/FD/XL



POWER INTEGRITY MEASUREMENTS: POWER RAIL NOISE, RIPPLE, etc.







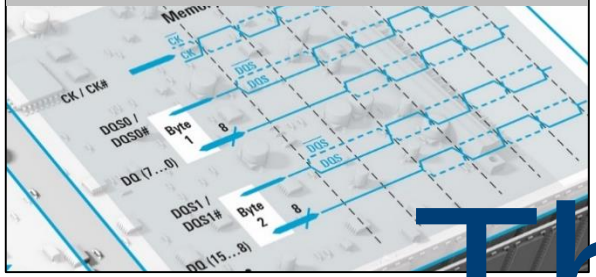
- Low noise and high resolution for power ripple
- Deep capture to look into slow drifts and response
- Spectrum capability to identify crosstalk, noise, …

POWER DELIVERY / POWER INTEGRITY TEST WITH MXO 5

4 / 8	channels and more	MORE channels to analyze multiphase buck converters and power-up / power-down sequencing
> 4.5 Million	wfms / sec	Instantly see MORE infrequent events
12 -bit	ADC 18-bit (HD-Mode)	MORE resolution on all sample rates
2 V	offset @ 0.5 mV/div	MORE resolution on power rail disturbance (DC meter functionality with power rail probes)
Digital	trigger	Trigger with MORE sensitivity and higher flexibility to define trigger conditions
> 45 k	FFT / sec	MORE FFTs with unmatched speed
500 Mpts	memory /ch	Capture even MORE time

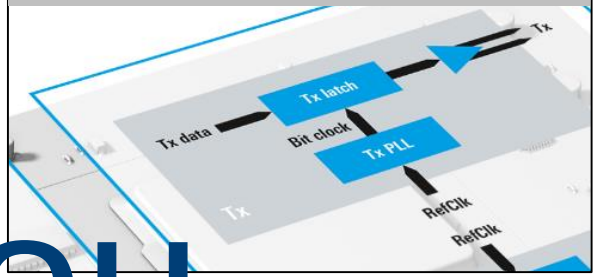
SIGNAL AND POWER INTEGRITY: CHALLENGES AND TEST SOLUTIONS

Signal Integrity: Interface Test

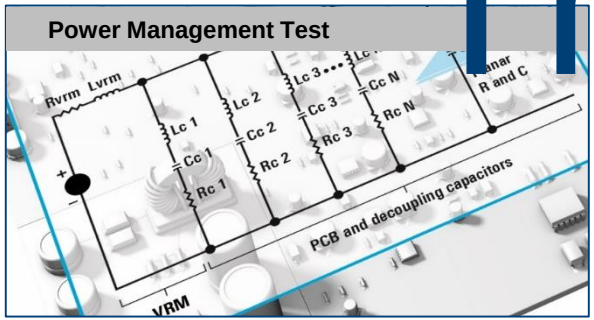


Signal Integrity: PCB and Interconnect Test

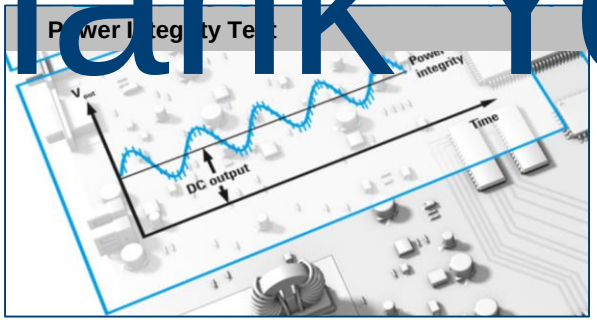
RefClk and SOC Test



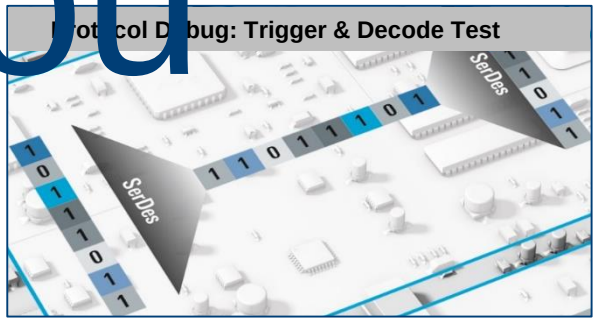
Power Management Test



Power Integrity Test



Protocol Debug: Trigger & Decode Test



Thank You